INDIUM-GALLIUM ARSENIDE SCHOTTKY BARRIERS

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CERTIFICATE

This is to certify that the thesis entitled 'Indium-Gallium Arsenide Schottky Barriers' by V.K. Handu is a record of work carried out under my supervision and has not been submitted elsewhere for a degree.

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ABSTRACT

In-GaAs Schottky barriers have been made by the vacuum evaporation of Indium onto chemically prepared n-GaAs at a pressure of 1×10^{-6} torr. Ohmic contacts to the samples have been made by alloying In-Au composition (90:10 percent by weight) at a temperature of 550°C for about 30 seconds. Barrier heights have been determined by using (i) Forward I-V characteristics, (ii) C-V measurement, and (iii) Photoelectric measurement. Barrier heights obtained by all these methods are in reasonably good agreement.

Photoelectric method of measurement has also been used to determine the image force dielectric constant. But agreement between theory and experiment is not satisfactory.

I-V characteristics of In-GaAs contacts have been thoroughly investigated. The diode current is described by

$$I = I_s(e^{qV/nkT} - 1).$$

Values of the parameter n lying between 1.06 to 1.1 have been obtained. n is found to vary with temperature.

An attempt has also been made to determine the surface state density and the position of the Fermi level at the surface of GaAs. For this purpose Schottky barriers were fabricated by using five other metals namely, Al, Au, Bi, Mg and Sb. A plot of the barrier height versus the metal work function was used to determine the surface state density and the position of the Fermi level. It is seen that the Fermi level of the surface states lies at one third of the energy gap above the valence band edge.

Chapter 1

INTRODUCTION

1.1 HISTORICAL INTRODUCTION

The credit for the earliest investigations on the metal-semiconductor rectifying contacts goes to a German physicist E.Braun who in 1874 noted the dependence of the total contact resistance on the polarity of the applied voltage and also on the surface conditions. Wilson[1], in 1931, presented the transport theory of semiconductors based on the band theory of solids. This theory was applied to study the properties of metal-semiconductor contacts. In 1938 Schottky[2] suggested that the potential barrier at the metal-semiconductor interface could exist because of the presence of the space-charges in the semiconductor alone and these charges were thought to arise from the presence of the metal. The model of metal-semiconductor contacts based on these considerations has been named after Schottky and the resulting barrier is called the Schottky barrier.

According to the simple theory[3] of Schottky, the barrier height at the metal-semiconductor interface, ϕ_{Bn}, is given by

$$\phi_{Bn} = \phi_m - X \qquad (1.1)$$

where ϕ_m is the work function of the metal and X is the electron affinity of the semiconductor. A two dimensional

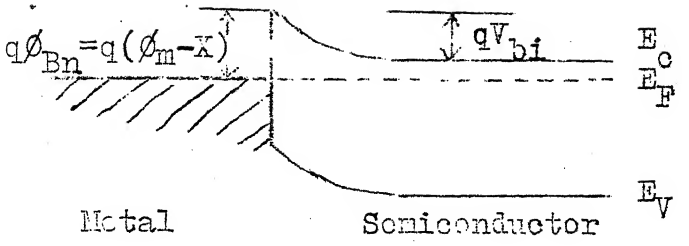

Figure 1.1 Energy band diagram of a metal-semiconductor contact.

representation of such a barrier is shown in Figure 1.1.

Although Schottky model predicts a barrier height ϕ_{Bn} dependent on metal work function, experiments performed on silicon and germanium showed ϕ_{Bn} to be largely independent of metal work function. These observations lead Bardeen in 1947 to propose an extension of the above theory by taking the effect of surface states[4] into consideration.

According to Bardeen's[4] theory if the density of semiconductor surface states having energies distributed in the band gap of the semiconductor is quite high, a double layer is formed at the free surface of the semiconductor even before bringing the metal into contact. This double layer consists of a net charge in the surface states and a space charge of opposite sign into the bulk of the semiconductor underneath the surface. Bardeen showed that such a double layer tends to make the contact properties almost independent of the work function of the contacted metal.

Spitzer and Mead[5] in 1963 and then again in 1964[6] as well as Cowley and Sze[7] have verified that gallium arsenide follows Bardeen's theory with the Fermi level at the surface pinned at about one third the band gap above the valence band edge. The same is also true about silicon and germanium[6]. The measurement of barrier height on some of the II-VI compound semiconductors such as CdS, however, showed that the barrier height varied in accordance with equation (1.1). These observations led to somewhat confusing situation about the origin of the barrier height. This confusion has been cleared by the work of Mead[8] who, after an extensive review of the experimental data, has divided the semiconductors in two categories: those having a large density of surface states and those having a small density of surface states. In his work Mead concludes that for all practical purposes materials like GaAs and Si, in which the barrier energies change only slightly with different metals, will be considered to fall in the surface-state determined catagory, although there is obviously some dependence upon the metal work function also, whereas II-VI compound semiconductors do not appear to have any substantial number of surface states and barrier height is determined largely by the metal work function.

1.2 APPLICATIONS OF SCHOTTKY BARRIERS

In recent years considerable interest has rekindled in the study of Schottky barrier contacts because of their applications in the microwave amplifiers, mixers and detector diodes as well as in metal-base and junction field-effect transistors[9]. Schottky barrier contacts have frequently been used in the semiconductor industry to measure the carrier concentration profiles of epitaxial layers. Also metal-semiconductor contact has been found to be a useful tool in the study of semiconductor surfaces which control the performance and stability of semiconductor devices. Recently reproducible and near ideal metal-semiconductor contacts have been fabricated on Si, GaAs, GaP and CdS with the help of the modern technology and improved vacuum techniques. Gallium arsenide Schottky barriers have proved particularly advantageous because high surface state density on GaAs (i) facilitates the reproducible fabrication of Schottky barriers, (ii) renders the diode properties relatively insensitive to the surface preparation thus simplifying the production technique and (iii) makes GaAs surfaces less prone to the instabilities that are common in Si and Ge.

1.3 METHODS OF FABRICATING SCHOTTKY BARRIERS ON GaAs

Spitzer and Mead[5-6], et.al. have used the conventional vacuum evaporation to fabricate Schottky barriers on vacuum cleaved and chemically prepared

n-GaAs surfaces. They found that the room temperature value of the barrier height for all metals (Au, Cu, Be, Ag, Pt, Al and Sn) with the exception of tin was between 0.8 and 0.98 eV and that the barrier height measurements showed an appreciable dependence on the method of surface preparation. An interesting feature of their results was that the barrier height obtained from the photoelectric measurement showed a tendency to be somewhat less than the barrier height obtained from capacity measurement.

Kahng[10], working independently at the Bell Telephone Laboratory, also reported his barrier height measurements on metal-GaAs Schottky barriers. He used the same metals as those used by Spitzer and Mead[5-6]. The values reported by Kahng are slightly different from the values reported by Spitzer and Mead. However, it is difficult to compare their results because the fabrication of the Schottky barriers have been done using different surface preparation techniques and different cleaning procedures.

Besides the vacuum evaporation technique, other methods have also been developed to fabricate the metal GaAs schottky barriers. One of these methods was developed by Crowell, Sarace and Sze[11] in 1967. They fabricated tungesten-GaAs schottky barriers by reacting tungesten-hexafluoride with GaAs surface in an argon atmosphere at temperatures between 325°C and 400°C. These workers reported the photoelectric measurement value of the barrier

height which was slightly higher than the capacity measured value of the barrier height. Incidently W-GaAs and Au-GaAs Schottky barriers have attained commercial importance.

As early as 1962, R. Williams[12] developed at RCA Laboratories a technique to make Sn-GaAs Schottky barriers by electroplating tin onto the etched GaAs surface. A modified technique has been used by Döbreck[13] to fabricate electrochemically deposited Schottky barrier contact on GaAs which had better noise characteristics. However, this paper reports the values of barrier heights for Au-GaAs and Cu-GaAs which are higher than the values given by Kahng[10] et.al. and also higher than those given by Mead and Spitzer[5-6] et.al.

More recently Ladd and Feucht[14] have reported the fabrication of GaAs Schottky barrier diodes by the fluxed wetting of tin and Indium. A barrier height value of 1.1 to 1.2 volts for In-1 percent Zn diodes on n-GaAs and a value of 0.7 to 0.8 volts for Sn diodes, also on n-GaAs, have been reported.

1.4 OBJECTIVES OF THE PRESENT WORK

The main purpose of the present work has been to fabricate good In-GaAs Schottky barriers and to study their properties. Indium was chosen because it is an inexpensive metal, is easily available and can also be used

to make ohmic contacts on GaAs. An attempt has also been made to study the distribution of surface states at the GaAs surface used in the fabrication of these Schottky barriers.

The work presented in this report is largely experimental. Chapter II of this work is devoted to the preparation and properties of single crystal GaAs. This has been done with the intention of knowing about GaAs as a semiconducting material and hence, laying a foundation for the systematic understanding of the devices fabricated on this material. Chapter III deals with the general theory of metal-semiconductor contacts. The knowledge of this theory is essential for the understanding of the present work. Chapter IV and V form the most important part of this report. Chapter IV deals with the ohmic contacts on GaAs and the measurement of various parameters of the bulk GaAs. Ohmic contacts are an important part of the device fabrication and so their study has been reported in detail. Chapter V reports on the fabrication of In-GaAs Schottky barriers. Various types of measurements performed on the fabricated devices have been described and the results of these measurements are compared. The possible errors that could arise in these measurements are discussed in detail. Chapter V also reports on the study of GaAs surface. The results obtained here are compared with the data available in the literature. Finally, in Chapter 6, the conclusion drawn from this work are presented and the possibility of In-GaAs Schottky barrier as a device for commercial applications is discussed.

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Chapter 2

PREPARATION AND PROPERTIES OF SINGLE CRYSTAL GALLIUM ARSENIDE

Gallium Arsenide is one of the III-V group compound semiconductors having the zinc-blende crystal structure. Its lattice may be considered as two interpenetrating face-centered cubic sub-lattices, one made up of gallium atoms and the other of arsenic atoms. The binding of atoms in GaAs is a mixture of ionic and covalent bonding.

2.1 PREPARATION AND DOPING

2.1.1 Preparation:

The simplest method of growing pure single crystals of gallium arsenide is by the Bridgeman[1] technique. Gallium arsenide crystals can also be pulled from the melt by the Czochralski technique[2]. The purest material made by these methods contain small quantities of silicon and oxygen and has a total impurity content of 10^{16} per cm^3 though neither of the impurities is present in such amounts in the starting elements. It appears that a reaction between the molten GaAs and the container (silica or graphite boats) causes the contamination.

To avoid contamination by the container, various workers have made crystals of gallium arsenide by floating-zone[3] technique. The total impurity content in ingots

treated by floating-zone technique is probably[4] near 10^{15} per cm^3.

Gallium arsenide crystals can be made from a solution of arsenic in gallium[5], and from a chemical reaction between gallium and arsenic trichloride[6] but these methods have found little use in commercial applications. Growth from the vapor phase is now commonly used for device fabrication, because single crystal layers of gallium arsenide can be formed by epitaxial growth[7] on gallium arsenide substrates. An undesirable feature or defect which is commonly found in layers of gallium arsenide grown by the vapor phase epitaxy[8] is the pyramid or hillock formation. Single crystal gallium arsenide formed by the liquid phase epitaxy[9] can also give excellent results in some device applications demanding highly doped epitaxial films free from any pyramid or hillock formation.

2.1.2 Doping of GaAs:

In general Groups I and II impurities act as acceptors in gallium arsenide and Groups IV and VI impurities as donors. The impurities of groups II and VI of the periodic table are substitutionally built into the sublattices of gallium and arsenic respectively. Thus Groups II and VI impurities act as acceptors and donors respectively in GaAs. Zinc and cadmium are the two most important acceptors since no departure from the substitutional acceptor character has been observed in these elements.

Magnesium from Group II is an exception. There are contradicting statements about its behaviour in GaAs. It has been indicated by various research workers that magnesium acts as a donor[10] (occupying an interstitial position) at low concentrations, and an acceptor[11] (occupying substitutional position) at high concentrations.

Among the elements of Group VI of the periodic table, selenium, tellurium and sulfur have been shown to be donors in GaAs. About oxygen, one only knows that it forms deep levels. Doping with oxygen is a convenient way of preparing gallium arsenide with a resistivity of 10^6 ohm-cms. or more, the material is known as semi-insulating GaAs[12]. It is made by heating gallium arsenide to a temperature of 1,150°C for 12 hours in an atmosphere of oxygen at 60 mm. pressure.

The behaviour of the Group IV impurities in GaAs is not as obvious as the behaviour of the Group II and VI impurities. The most favourable explanation[13] that has been given is that Group IV atoms at low concentrations tend to replace neighbouring gallium and arsenic atoms and result in electrically neutral centres. Silicon, germanium, tin and lead[14] are all soluble in gallium arsenide upto 0.5 percent (atomic) but the maximum number of donors which can be produced by doping from the melt is less than 10^{19} per cm^3.

Impurities from Groups III and V behave as electrically neutral centers in gallium arsenide. When large quantities of the impurity are added, a mixed crystal of two Groups III-V compounds is formed.

Acceptors like zinc, manganese and cadmium, and donors like tin, selenium and sulfur, have been diffused into gallium arsenide although all of them do not appear to obey the elementary diffusion laws. Goldstein[14] has measured diffusion of selenium and sulfur in GaAs and finds that Fick's law is obeyed, though there is a tendency for low melting point glasses to be formed on the gallium arsenide surface during the diffusion. Cunnell and Gooch have shown that the diffusion of both zinc[15] and cadmium[16] is anomalous. Above 800°C the diffusion coefficient of zinc is concentration dependent and Fick's law is not obeyed. In case of cadmium, Fick's law is obeyed for distances upto 25 microns below the surface. Beyond this region the concentration rises gradually and then remains constant for a distance of 1 mm. or more. Copper diffuses rapidly into gallium arsenide, the diffusion coefficient being near 10^{-6} cm^2 $sec.^{-1}$ at 1,000°C. This is an apparant diffusion coefficient, for Fick's law is not obeyed.

2.2 BULK ELECTRICAL AND RELATED PROPERTIES

The probable band structure of gallium arsenide is summarized in Figure 2.1. The direct band gap has been deduced[17] from infra-red absorption and is 1.52 eV at

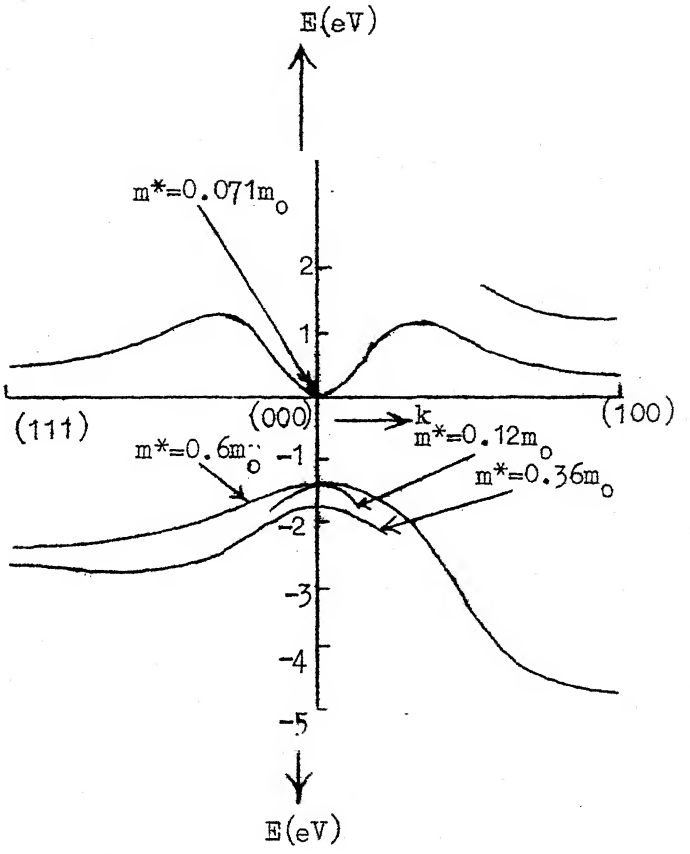

Figure 2.1 The band structure of gallium arsenide.

0°K and about 1.4 eV at room temperature. Experiments show that the electron effective mass in gallium arsenide is low. Hole effective masses are less established. The light-hole mass and the mass in the split-off valence band are found to be 0.12 m_o and 0.36 m_o respectively, where m_o is the free electron mass. It has also been found that the heavy-hole mass is about six times the light hole mass[18].

Some of the important properties of gallium arsenide are listed in Table 2.1. The mobility of electrons in semiconducting gallium arsenide is found to be greater than 5,000 cm^2/V-sec. The best available values[19] reported are:

electron mobility = 8,500 cm^2/V-sec.
hole mobility = 435 cm^2/V-sec.] at 300°K;

and electron mobility = 2,2000cm^2/V-sec. at 72°K.

The mobility gives a T^{-2} dependence[20] on temperature which is the best one can get in III-V compounds. The dependence of mobility on carrier concentration in case of semiconducting gallium arsenide is shown in Figures 2.2 and 2.3.

The wide band gap and high electron mobility extends the range of operation of gallium arsenide devices to higher temperatures and higher frequencies. The wide band gap also makes it possible to produce semi-insulating gallium arsenide which can be used for isolation purposes.

Studies made on the optical properties of gallium arsenide show that the vibration spectrum has five branches[21],

TABLE 2.1

Properties of GaAs at 300°K

Atoms/cm^3	2.21×10^{22}
Atomic weight	144.63
Crystal structure	zinc blende
Lattice constant (A^o)	5.6534
Melting point (^oC)	1238
Density ($gms./cm^3$)	5.32
Dielectric constant	10.9
Electron affinity[26] (eV) ($N_D, N_A = 2 \times 10^{16} cm^{-3}$)	4.07
Work function[26] (eV) ($N_D, N_A = 2 \times 10^{16} cm^{-3}$)	4.71
Energy gap (eV) at 300°K	1.43
Breakdown field (V/cm.)	4×10^5
Effective density of states in conduction band, N_C (cm^{-3})	4.7×10^{17}
Effective density of states in valence band, N_V (cm^{-3})	7×10^{18}
Intrinsic carrier concentration (cm^{-3})	1.1×10^7
Effective mass m*, electrons	0.068 m_o
holes	0.12 m_o, 0.5 m_o
Minority carrier lifetime (sec.)	10^{-8}
Mobility (Drift) electrons (cm^2/V-sec.)	8,500
holes	400

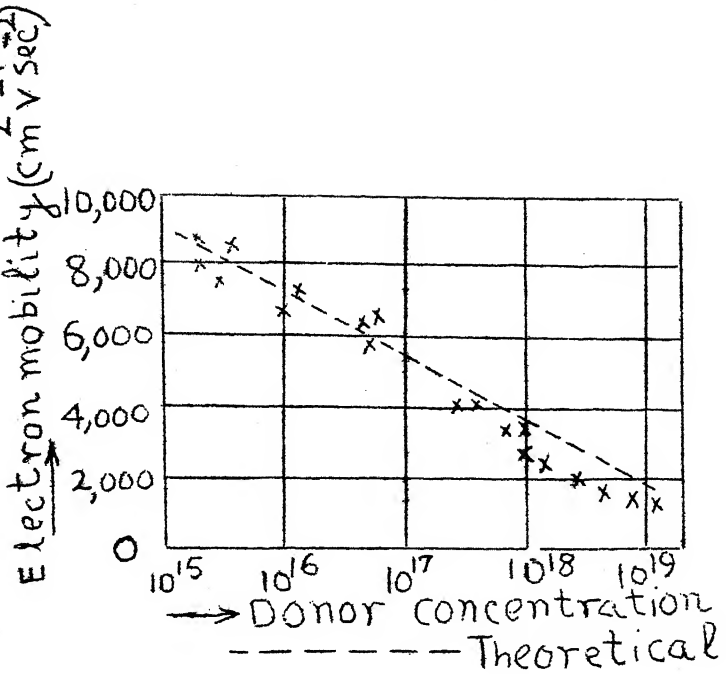

Figure 2.2 The dependence of electron mobility on donor concentration[22].

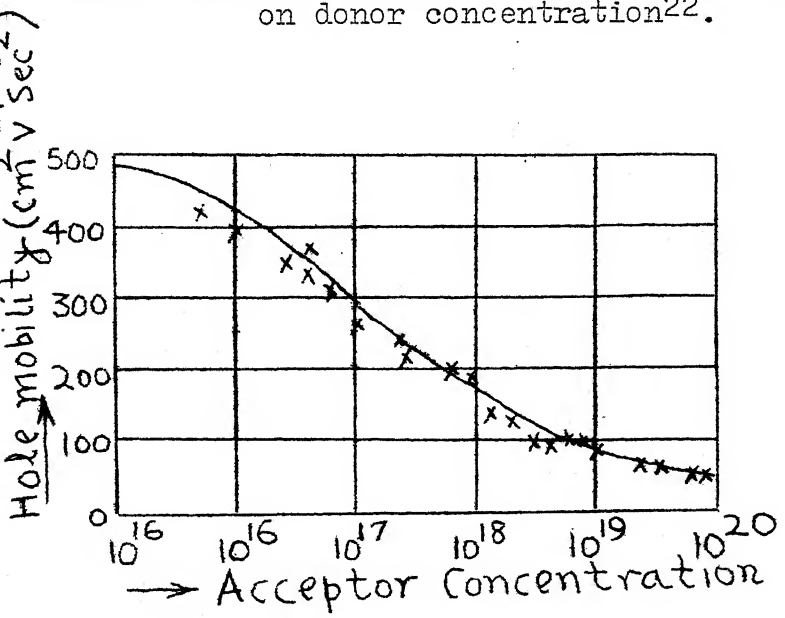

Figure 2.3 The dependence of hole mobility on acceptor concentration[23].

there being two characteristic transverse optical frequencies.

The minority carrier lifetime in the samples of gallium arsenide is always less than a microsecond. Gallium arsenide contains appreciable quantities of a number of impurities and one might expect that some of these would act as recombination centers, like copper or nickel in silicon. The direct electron-hole recombination can be another important process-limiting carrier lifetime. Since the conduction band minimum and valence band maximum occur at the same value of k in E-k diagram of GaAs, the energy released by hole and electron recombination is emitted as radiation. This property of GaAs has led to the discovery of semiconductor laser and other electroluminiscent devices.

2.3 SURFACE PROPERTIES

The surface of gallium arsenide, although similar in many respect to germanium and silicon, has properties which may introduce marked differences of surface behaviour. A thin plate of gallium arsenide cut parallel to the (111) plane has, ideally, one face consisting entirely of gallium atoms (A face) and the other of arsenic atoms(B face). These faces have different chemical properties and may have different electrical properties. Experiments performed on n and p type GaAs have shown that there are active surface traps in the range of 10^{11}-10^{12} cm^{-2}

situated near the Fermi level. Both n and p type materials have depletion layers at the surface when the material is etched with 3:2:1 (HNO_3:H_2O:HF(40 percent)) etch. When SiO_2 is deposited on etched surfaces[24] of GaAs, again the surfaces have been found to have depletion layers with surface barriers in the range of 0.2 - 0.3 V and surface trap density about 7×10^{11} cm^{-2}.

The potential barrier on n-type GaAs is probably about 21 kT/q in ozone. On p-type it is at least 8kT/q in nitrogen and may be a good deal more. The surfaces are sensitive to ambient gases but not strongly so, and there is evidence of a slow relaxation phenomenon[25] in the presence of light. No clear difference has been observed between A and B faces on the (111) plane.

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Chapter 3

THEORY OF METAL-SEMICONDUCTOR CONTACTS

3.1 INTRODUCTION

In this chapter, the basic theory of metal-semiconductor contacts is presented and the origin of the barrier height is explained. Before discussing this topic, it would be appropriate to define some of the basic quantities of which frequent use is made in this work.

Figure 3.1(a) shows the energy band diagram of an n-type semiconductor. In this diagram the vacuum level is defined as the energy level at which an electron is at rest outside the crystal and does not experience any force from the crystal lattice. At the vacuum level the electron, thus, behaves like a free electron in vacuum.

Work Function:

For a metal or a semiconductor the minimum energy required to take an electron from the Fermi level to the vacuum level is defined as the work function.

Work function of metals is of the order of a few electron volts and varies between 1.93 eV (caesium) and 6.37 eV (platinum). Work function of semiconductor depends upon the concentration of impurities in the semiconductor.

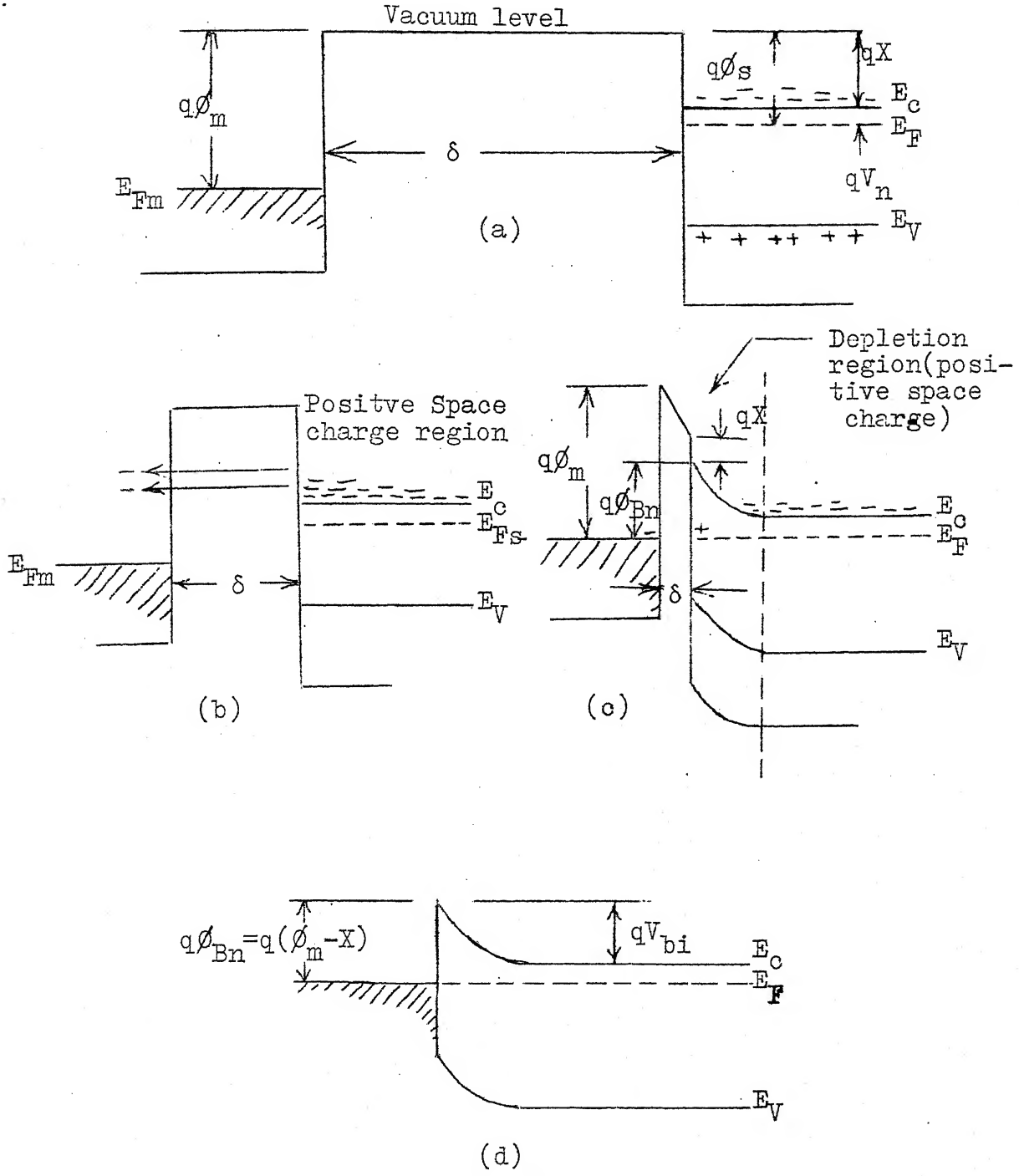


Figure 3.1: Energy band diagrams of ideal metal-semiconductor rectifying contact.

Electron Affinity:

The energy difference between the vacuum level and the bottom of the conduction band is called the electron affinity.

3.2 CONTACT PROBLEM

When two metals having different work functions are brought into contact with one another, a brief transient current flow takes place which transfers electrons from the metal with the smaller work function to the one with the larger work function, thereby generating an equilibrium contact potential difference between the two. The properties of metal-semiconductor contacts can be inferred using somewhat the same line of reasoning as those of metal-metal contact.

3.2.1 Ideal Metal-Semiconductor Contact:

Let us consider the contact between a metal with work function $q\phi_m$ and an n-type semiconductor with work function $q\phi_s$. When the two are brought into intimate contact with each other electrons flow from the lower work function side to the higher work function side till the thermodynamic equilibrium is achieved and a potential difference $(\phi_m - \phi_s)$ appears across the semiconductor. The work function of the metal can be smaller or larger than the work function of the semiconductor. Thus two cases exist:

(i) $\phi_m > \phi_s$; and

(ii) $\phi_m < \phi_s$.

3.2.2 Ohmic and Rectifying Contacts:

Figure 3.1 shows the situation which arises at the contact interface between a metal and an n-type semiconductor when the work function of the metal $q\phi_m$ is greater than that of the semiconductor $q\phi_s$. In Figure 3.1(a) the metal and semiconductor are not in contact and the system is not in thermal equilibrium. When the two are brought closer to each other, the electrons will flow from the semiconductor to the metal, see Figure 3.1(b), till electronic equilibrium is established and the two Fermi levels on both sides line up. Figure 3.1(c) shows that the Fermi level in the semiconductor has lowered by an amount equal to the difference between the work functions. As can be seen from this figure, the barrier seen from the semiconductor side will be

$$q(\phi_m - \phi_s) = q\phi_m - q(X - V_n) = qV_{bi}$$

where X is the electron affinity, and V_n is the difference between the Fermi level and the lower end of the conduction band and is dependent upon the impurity concentration in the semiconductor. V_{bi} is called the contact potential difference or the built-in voltage of the metal-semiconductor contact. The barrier seen from the metal side on the other hand is $q(\phi_m - X)$.

As the distance between the metal and semiconductor, denoted by δ, decreases an increasing negative charge is built up at the metal surface because more electrons will flow from the semiconductor into the metal. An equal and

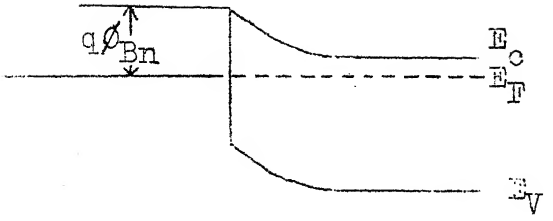
opposite charge (positive) must exist in the semiconductor. Thus the net carrier density near the surface of the semiconductor is reduced from its bulk value. As the surface layer is depleted of electrons near the surface it is referred to as depletion region.

When δ is small enough to be comparable with the interatomic distances, the gap becomes transparent to electrons and we obtain the limiting case as shown in Figure 3.1(d). At its maximum height, the barrier seen by the carriers from the metal side is known as metal-semiconductor barrier height given by:

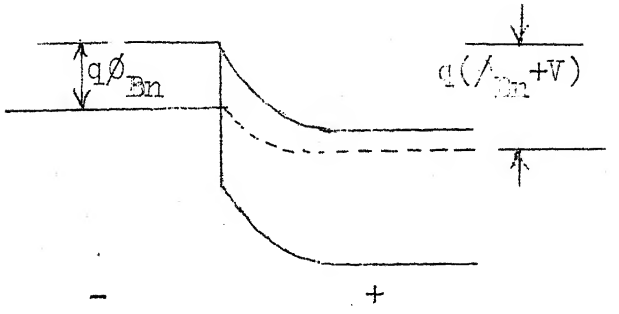
$$q\phi_{Bn} = q(\phi_m - X) \qquad (3.1)$$

Equation (3.1) is a somewhat ideal relationship because it neglects the presence of electric field at the metal semiconductor interface and also neglects the image force[1] on the emitted electron. The combined result of both these effects is to reduce the barrier height by an amount $\partial\phi$ (Appendix I) where $\partial\phi$ is the image force barrier lowering.

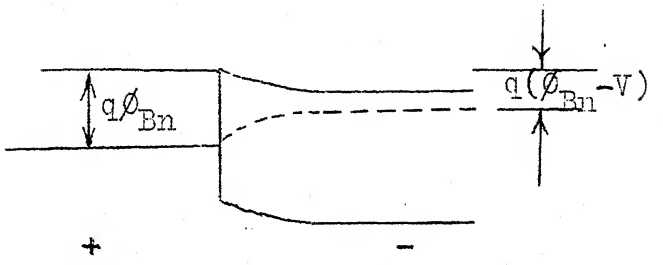
The metal-semiconductor contact depicted in Figure 3.1 is obviously a rectifying contact, also known as Schottky barrier contact, because the potential barrier obstructs the flow of electrons across the interface more in one direction than in the other. Figure 3.2 is drawn to explain the rectifying characteristics of such a contact. In equilibrium (Figure 3.2(a)) a barrier ϕ_{Bn} exists at the



(a) Thermal equilibrium



(b) Reverse bias



(c) Forward bias

Figure 3.2: Energy band diagram of metal-n-type semiconductor contact under different biasing conditions.

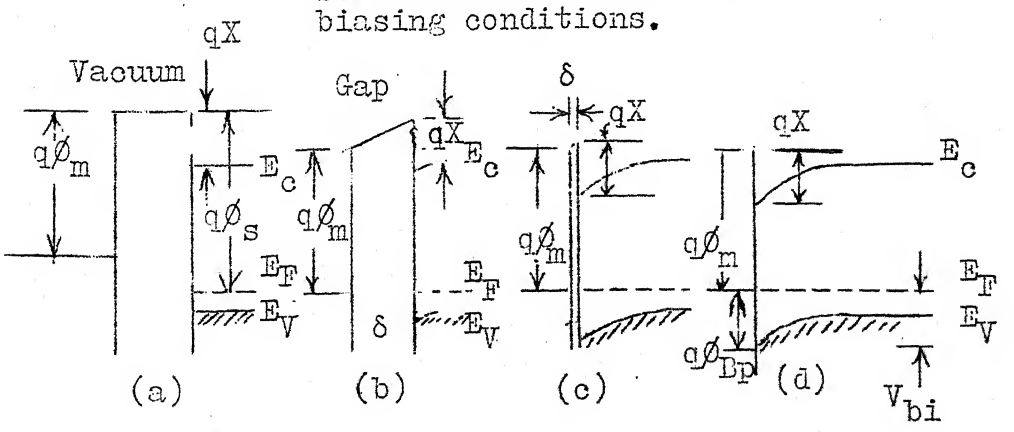


Figure 3.3 Energy band diagram of an ideal metal-p-type semiconductor contact.

interface as discussed above. Some electrons in the metal have sufficient energy to overcome this barrier and flow into the semiconductor. Similarly, some electrons in the semiconductor have sufficient energy to reach the metal and, at equilibrium, these two oppositely directed electron currents are equal. If an external potential is applied between the metal and the semiconductor, the equilibrium condition is disturbed. When the semiconductor is made positive as shown in Figure 3.2(b), the height of the barrier is increased to $q(\phi_{Bn} + V)$, where V is the external potential. Since the barrier height as seen from the semiconductor side is increased, few electrons can now flow from the semiconductor to the metal. The height of the barrier viewed from the metal is unchanged so that the current flow from the metal to the semiconductor is the same. Thus there is a net current flow from the metal to the semiconductor. When the polarity of the external potential is reversed as seen in Figure 3.2(c), the barrier height on the semiconductor side is reduced to $q(\phi_{Bn}-V)$ and the current from the semiconductor is increased. This results in a net current into the metal. Since the electron current from the metal is unaffected by the external potential, the rectifying characteristics of the contact depend only on the current flowing from the semiconductor. The two cases discussed above are called the reverse and forward biasing, respectively, of the metal-semiconductor contact.

For an ideal contact between a metal and a p-type semiconductor, the barrier height, $q\phi_{Bp}$, is given by, as seen in Figure 3.3,

$$q\phi_{Bp} = E_g - q(\phi_m - X) \qquad (3.2)$$

where E_g is the band gap of the semiconductor.

From equations (3.1) and (3.2) we can write

$$q(\phi_{Bn} + \phi_{Bp}) = E_g ,$$

that is for a given semiconductor and for any metal the sum of the barrier heights on n-type and p-type substrates is thus equal to the band gap.

Figure 3.4(a) shows the case of a metal and n-semiconductor contact when $\phi_m < \phi_s$. Here the electrons flow from the metal into the semiconductor. Thus the semiconductor acquires a negative charge, the metal a positive one and the bands bend downwards at the surface. As a result, instead of a depletion layer, an accumulation layer of electrons is formed. This contact, therefore, acts as an ohmic contact since no barrier exists to stop the flow of electrons in either direction as can be seen in the energy band diagram of Figure 3.4(b).

3.3 EFFECT OF SURFACE STATES[2] ON RECTIFYING PROPERTIES OF METAL-SEMICONDUCTOR CONTACTS

Let us consider now an n-type semiconductor having a considerable number of acceptor type surface states whose density and distribution in energy is shown in Figure 3.5.

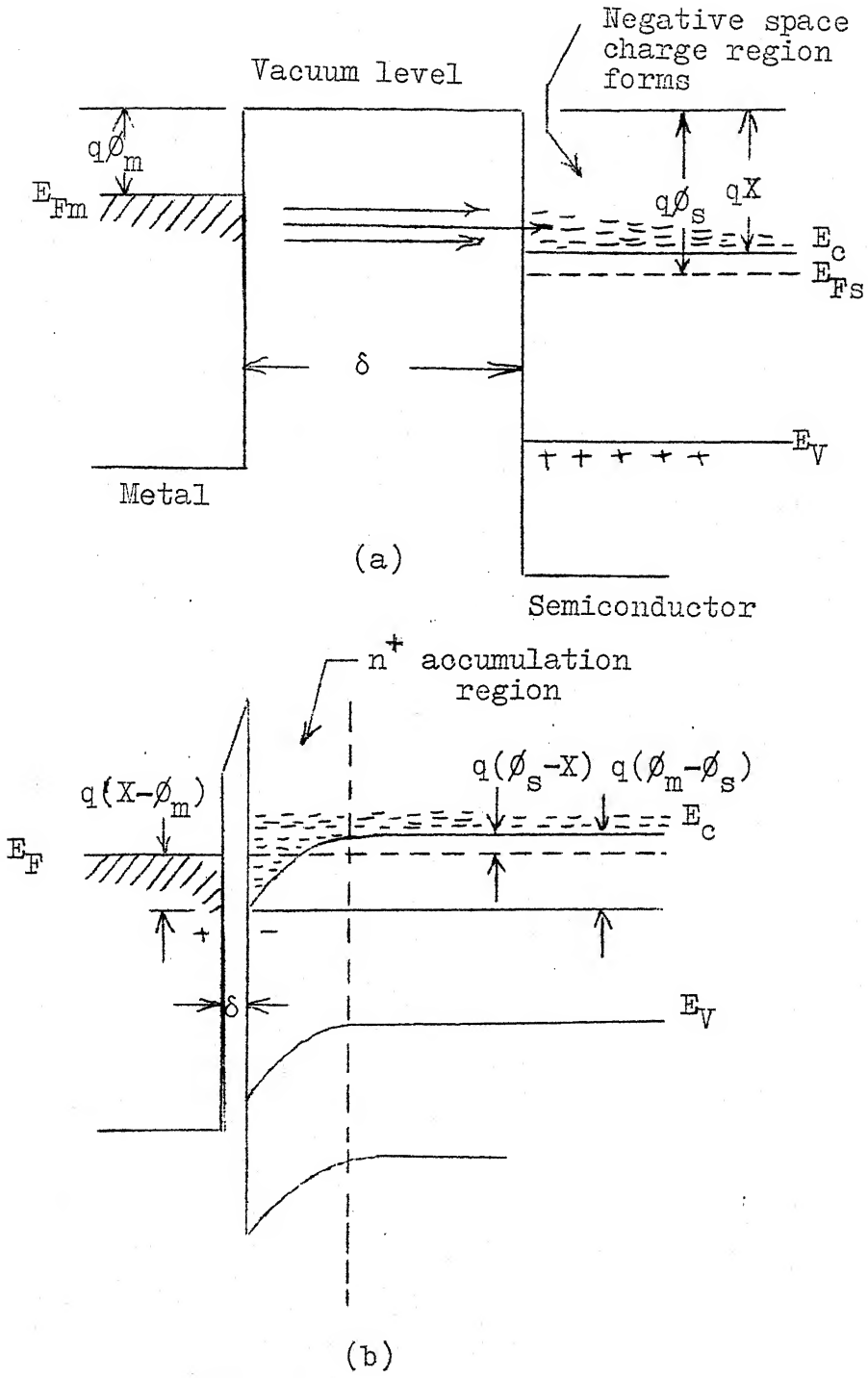


Figure 3.4: Energy band diagram of an ideal metal-n-type semiconductor contact when $\phi_m<\phi_s$.

When there is no contact existing between the metal and the semiconductor, the surface states will be filled upto the Fermi level creating a positive space charge layer in the bulk of the semiconductor. When a metal, whose work function ϕ_m is less than the work function of semiconductor, is made to approach such a semiconductor surface, the condition existing at the interface will now be different from the cases considered in Section 3.2. Had there been no surface states this metal would have produced an accumulation layer in the semiconductor as explained earlier. Since the surface states are existing and as the metal approaches the semiconductor, the electrons start flowing from the metal into the semiconductor. If the density of surface states is substantially large, the surface states themselves will accomodate all the electrons and the final state of the system will be as depicted in Figure 3.5(b). The situation inside the semiconductor is essentially the same as in Figure 3.5(a) except that the Fermi level is a bit higher with respect to the surface state distribution. This has resulted in a small change $d\phi_{Bn}$ in the barrier height which will be very small if the surface state density is sufficiently large. The depletion region inside the semiconductor remains almost unaffected. The presence of acceptor type surface states, thus, has converted an ohmic contact into a rectifying contact with barrier height determined predominantly by the surface states.

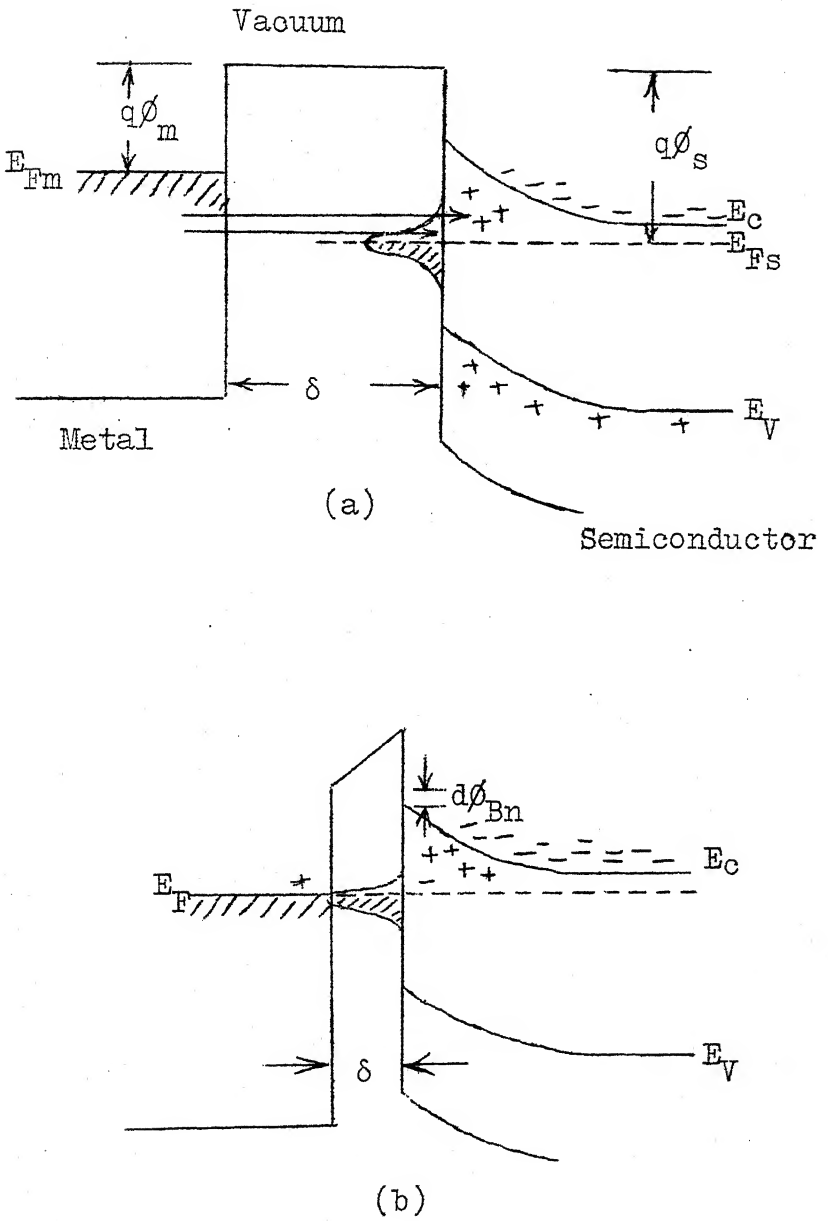
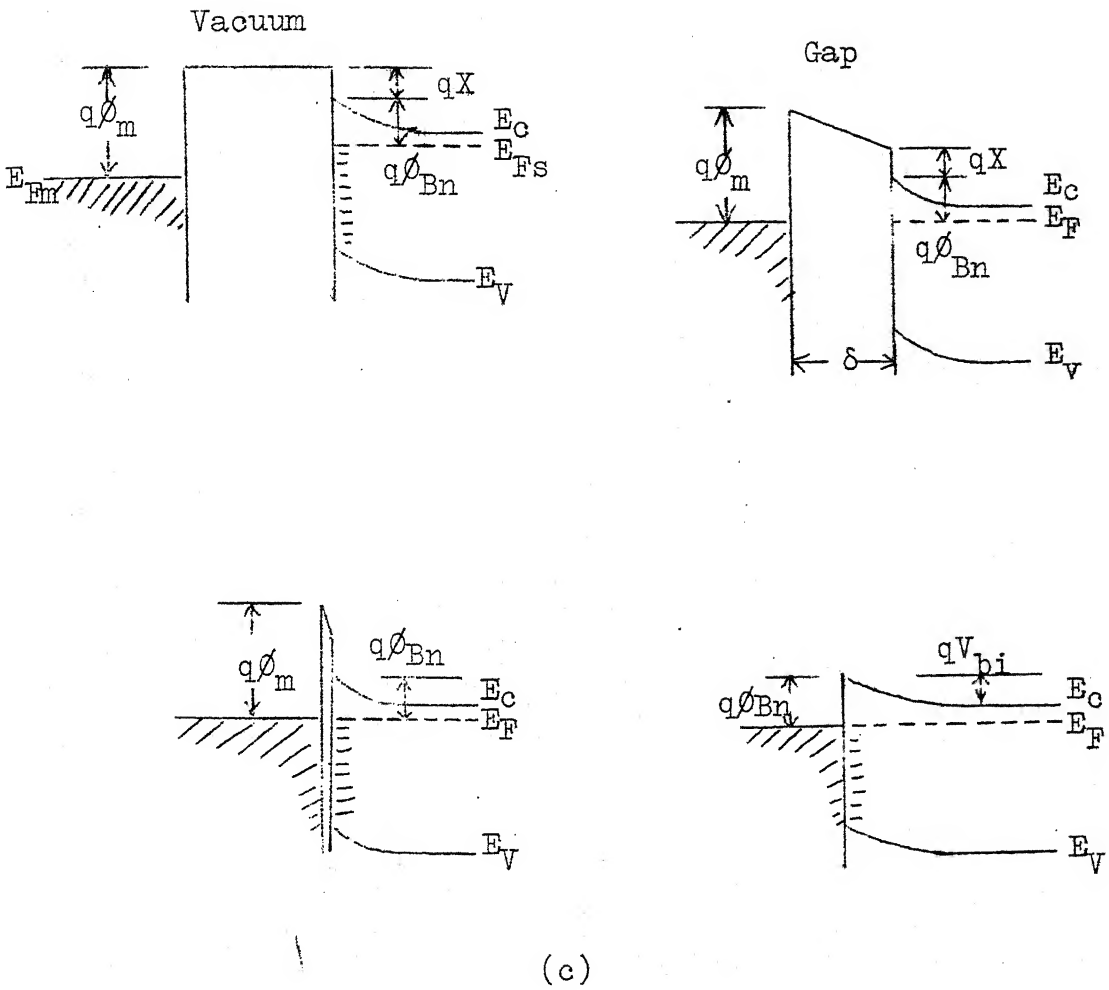


Figure 3.5: Energy band diagrams showing successive stages in the establishment of equilibrium between a metal and semiconductor with surface states when $\phi_m < \phi_s$.



(c)

Figure 3.5: Energy band diagrams showing successive stages in the establishment of equilibrium between a metal and semiconductor with surface states when $\phi_m > \phi_s$.

Consider the same situation except that the work function of the metal exceeds that of the semiconductor, the barrier height change $d\phi_{Bn}$ is of opposite sign and the flow of electrons from the surface states to the metal lowers the Fermi level with respect to the surface state distribution. Again the rectifying properties are virtually unaffected.

Figure 3.5(c) illustrates the successive stages in the establishment of equilibrium between a metal and n-type semiconductor with surface state when $\phi_m > \phi_s$. The rectification characteristics are seen to be practially independent of the relative values of the two work functions.

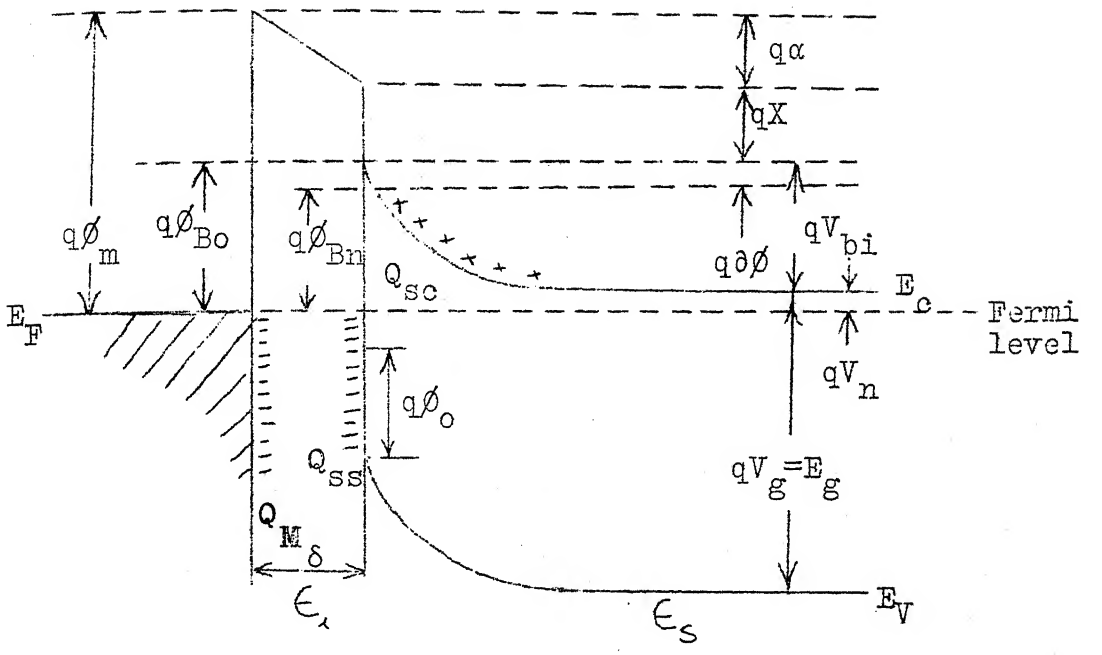
3.4 BARRIER HEIGHT THEORY[3]

A general expression for the barrier height has been obtained by making the following assumptions:

(i) any interfacial layer between the metal and the semiconductor is transparent to electrons and can withstand potential across it, and

(ii) the surface-state density is just the function of the semiconductor and is independent of the metal.

A detailed energy band diagram of a rectifying metal-semiconductor contact is shown in Figure 3.6. We consider the semiconductor with a constant acceptor like surface state density of D_s states/cm^2/eV. Then Q_{ss}, the charge in the surface states, is given by



ϕ_m = work function of metal .
ϕ_{Bn} = barrier height of metal-semiconductor contact
ϕ_{Bo} = value of ϕ_{Bn} at zero electric field
ϕ_o = energy level at the surface
$\partial\phi$ = image force barrier lowering
α = potential across interfacial layer
X = electron affinity of semiconductor
V_{bi} = built-in potential
ϵ_s = permittivity of semiconductor
ϵ_i = permittivity of interfacial layer
δ = thickness of interfacial layer
Q_{sc} = space-charge density in semiconductor
Q_{ss} = Surface-charge density of semiconductor
Q_M = Space-charge density of metal.

Figure 3.6 Detailed energy band diagram of a metal-n-type semiconductor contact with an interfacial layer of the order of atomic distance.

$$Q_{ss} = -qD_s \times \text{energy difference between } E_F \text{ and } q\phi_o$$

$$= -qD_s(E_F - q\phi_o)$$

Now $E_F = E_g - q\phi_o$

$$= (E_g - q\phi_B - q\partial\phi)$$

so that

$$Q_{ss} = -qD_s(E_g - q\phi_B - q\partial\phi - q\phi_o) \qquad (3.3)$$

The space charge in the depletion layer of the semiconductor is[1]

$$Q_{sc} = qN_D W = \left(2\epsilon_s qN_D\left(V_i - V_a - \frac{kT}{q}\right)\right)^{1/2}$$

In thermal equilibrium condition $V_a = 0$, and

$$Q_{sc} = \left(2\epsilon_s qN_D\left(V_i - \frac{kT}{q}\right)\right)^{1/2}$$

$$= \left(2\epsilon_s qN_D(\phi_B - V_n + \partial\phi - kT)\right)^{1/2} \qquad (3.4)$$

The potential across the interfacial layer can be obtained by applying Gauss's law to the surface charge in the metal and the semiconductor

$$\epsilon_i E = \epsilon_i \frac{\alpha}{\delta} = -Q_M \qquad (3.5)$$

or

$$= -\frac{Q_M}{\epsilon_i}\delta$$

Also from Figure 3.6 we see that

$$\alpha = \phi_m - (\phi_B + \partial\phi + X) \qquad (3.6)$$

From equations (3.5) and (3.6), we get

$$Q_M = -\frac{\epsilon_i}{\delta}(\phi_m - (\phi_B + \partial\phi + X)) \qquad (3.7)$$

If there is no charge in the interfacial layer then we must have

$$Q_{ss} + Q_{sc} + Q_M = 0 \qquad (3.8)$$

Substituting for Q_{ss}, Q_{sc} and Q_M and solving for ϕ_{Bn}, we obtain

$$\phi_{Bn} = \left[C_2(\phi_m - X) + (1-C_2)\left(\frac{E_g}{q} - \phi_o\right) - \partial\phi \right] + \left\{ \frac{C_2^2 C_1}{2} - C_2^{3/2} \left[C_1(\phi_m - X) + (1-C_2)\frac{C_1}{C_2}\left(\frac{E_g}{q} - \phi_o\right) - \frac{C_1}{C_2}\left(V_n + \frac{kT}{q}\right) + \frac{C_2 C_1^2}{4} \right]^{1/2} \right\} \qquad (3.9)$$

where

$$C_1 = \frac{2q\,\epsilon_s N_D \delta^2}{\epsilon_i^2} \qquad (3.10)$$

and

$$C_2 = \frac{\epsilon_i}{\epsilon_i + q^2 \delta D_s} \qquad (3.11)$$

Now, if C_1 is small and the second term in equation (3.9) is less than 40 mV, neglecting this term, we obtain

$$\phi_{Bn} = C_2(\phi_m - X) + (1-C_2)\left(\frac{E_g}{q} - \phi_o\right) - \partial\phi \qquad (3.12)$$

or

$$\phi_{Bn} = C_2 \phi_m + C_3 \qquad (3.13)$$

From equation (3.11)

$$D_s = \frac{(1-C_2)\epsilon_i}{C_2 \delta q^2} \qquad (3.14)$$

For $\delta = 2$ to $6\ A^o$; and $\epsilon_i \simeq \epsilon_o$, we obtain

$$D_s \simeq 1.1 \times 10^{13}(1-C_2)/C_2 \text{ states per cm}^2 \text{ per eV}$$

Two limiting cases can be obtained directly from equation (3.12):

(a) when D_s is very low so that $D_s \to 0$, then

$$\phi_{Bn} = (\phi_m - X) - \partial\phi \qquad (3.15)$$

which is identical to equation (3.1) except for $\partial\phi$.

(b) when D_s is very large so that $D_s \to \infty$, then

$$\phi_{Bn} = (\frac{E_g}{q} - \phi_o) - \partial\phi$$

or $$q\phi_{Bn} = (E_g - q\,\phi_o) - q\,\partial\phi \qquad (3.16)$$

In the case (b) the Fermi level at the interface is pinned at ϕ_o above the valence band and the barrier height is independent of ϕ_m but is determined entirely by ϕ_o and hence by the surface properties of the semiconductor.

Thus equations (3.15) and (3.16) tell us that the barrier height depends upon the metal work function

when the density of surface states is negligible, and the barrier height is exclusively dependent upon the surface properties of the semiconductor when the density of surface states in the semiconductor is large. When the theoretical expression given by equation (3.13) is compared to the experimentally determined available data[3] of ϕ_{Bn} vs. ϕ_m for Si, GaP, GaAs and CdS, it has been seen that the best straight-line fit is obtained in GaP and hence the calculations of ϕ_o and D_s can probably be considered reliable for this case.

The parameter C_2 in the theoretical expression of equation (3.13) is found to range from 0.07 for GaAs[4] having considerably large number of surface states to almost unity for CdS[5] having, ideally, negligible density of surface states. These data indicate the weak and strong dependence of the barrier height on the metal work function for GaAs and CdS, respectively.

The value of ϕ_o has been found to be roughly one third of the respective band gap energies for Si, GaAs and GaP[3] and the surface state density for these semiconductors is found to be in the range of $10^{13} - 10^{14}$ states per cm^2 per eV.

An alternative graphic method to calculate the barrier height has been given by Turner and Rhoderick[6]. Again referring to Figure 3.6,

$$- Q_M = Q_{ss} + Q_{sc}$$

where

$$Q_{ss} = -qD_s[\, E_g - q\phi_B - q\partial\phi - q\phi_o \,], \qquad (3.3)$$

$$Q_{sc} = (2\epsilon_s q\, N_D(V_i - \frac{kT}{q}))^{1/2}, \qquad (3.4)$$

and $$Q_M = -\frac{\epsilon_i}{\delta}[\, \phi_m - (\phi_B + \partial\phi + X) \,]. \qquad (3.7)$$

The equations (3.3), (3.4) and (3.7) can also be written in terms of the build-in potential V_{bi}[7] as follows:

$$Q_{ss} = -qD_s(E_g - qV_n - q\phi_o - q\, V_{bi}) \qquad (3.17)$$

$$Q_{sc} = (2q\epsilon_s\, N_D\, V_{bi})^{1/2} \qquad (3.18)$$

and $$Q_M = -\frac{\epsilon_i}{\delta}[\, \phi_m - X - V_n - V_{bi} \,] \qquad (3.19)$$

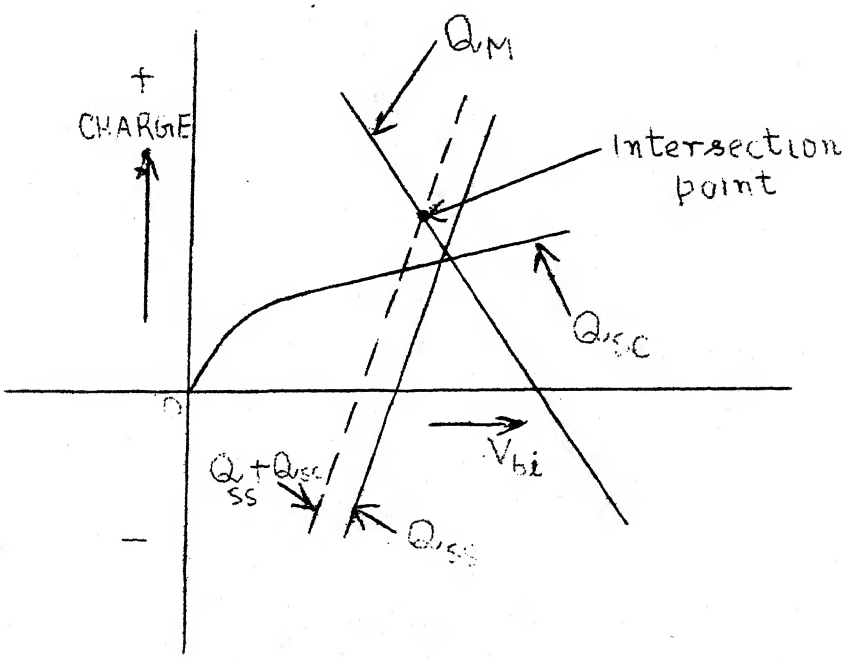


Figure 3.7 Graphical representation of Q vs. V_{bi} relationships at metal semiconductor surfaces.

If we plot $-Q_M$, Q_{sc}, Q_{ss} and hence $Q_{sc} + Q_{ss}$ on the same graph as a function of V_{bi}, then the intersection of $(-Q_M)$ and $(Q_{ss}+Q_{sc})$ can give us one particular value of $(-Q_M)$ corresponding to a particular value of V_{bi}. Since we know Q_M, V_{bi} can be calculated from equation (3.19) for the particular value of δ, ϵ_i, D_S, ϵ_s and ϕ_m. If N_D is also known, then the barrier height can be calculated.

3.5 MEASUREMENT OF BARRIER HEIGHT

The barrier height, ϕ_{Bn}, of a metal-semiconductor contact can be measured by either of the following methods:

(i) Measurement of forward I-V characteristics,
(ii) C-V measurement, and
(iii)Photoelectric measurement.

These methods are now described.

3.5.1 Forward I-V Characteristics:

The total current in a metal-semiconductor diode is given by[7]

$$I = I_s(e^{qV/nkT} - 1) \qquad (3.20)$$

where $$I_s = A^* T^2 \exp(-\frac{q\phi_{Bn}}{kT})$$

$$= A^* T^2 \exp(-q(\phi_{Bo} - \partial\phi)/kT), \qquad (3.21)$$

A^* being the effective Richardson constant in equation(3.21). Since both A^* and $\partial\phi$ are functions of voltage, the I-V characteristics for $V > kT/q$ is given by

$$I \propto \exp(qV/nkT)$$

where the parameter n is given by

$$n = \frac{q}{kT} \frac{\partial V}{\partial \ln(J)} \qquad (3.22)$$

$$= \left[1 + \frac{\partial(\partial \phi)}{\partial V} + \frac{kT}{q} \frac{\partial(\ln A^*)}{\partial V} \right]^{-1} \qquad (3.23)$$

The parameter n should be unity for an ideal Schottky barrier diode. For practical Schottky barriers, values of n are found to be slightly larger than unity. For example n = 1.02 for W-GaAs[8] and n = 1.04 for Au - Si[8] Schottky barriers have been reported.

The value of I_s can be obtained by extrapolating the log I vs. V plot to V = 0 and the barrier height can be obtained from, see Figure 3.8(a),

$$\phi_{Bn} = \frac{kT}{q} \ln\left(\frac{A^* T^2}{J_s}\right) \qquad (3.24)$$

Also, using equation (3.21), we get

$$\left(\frac{I_s}{T^2}\right) = A^* \exp\left(\frac{-q\phi_{Bn}}{kT}\right)$$

or $$\phi_{Bn} = -\frac{k}{q} \frac{d[\log(I_s/T^2)]}{d[1/T]} \qquad (3.25)$$

Thus if we plot $\log\left(\frac{I_s}{T^2}\right)$ vs. $\frac{1}{T}$ and substitute the value of the slope obtained from equation (3.25), see Figure 3.8(b), we will get the value of the barrier height. This is an alternate method of finding the barrier height from the temperature dependence of forward I-V characteristics.

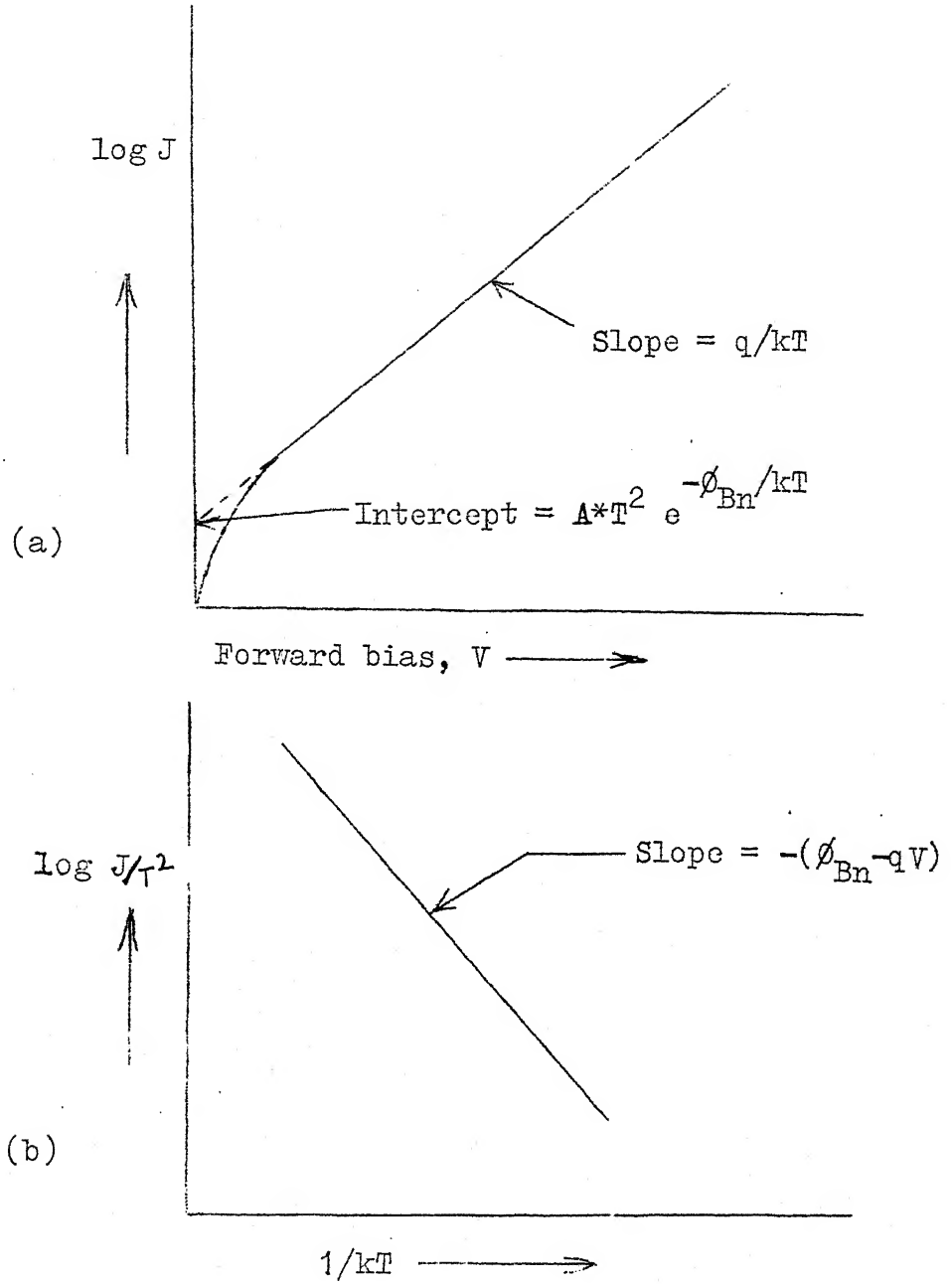


Figure 3.8: (a) I-V characteristics of forward biased metal-semiconductor contact.

(b) Activation energy plot of forward biased metal-semiconductor contact.

3.5.2 C-V Measurement:

The barrier height can also be determined by the capacitance measurement. When a small a-c voltage is superimposed upon d-c bias, charges of one sign are induced on the metal surface and charges of opposite sign in the semiconductor. The relationship between the capacitance C and the applied voltage V is given by[9], when the semiconductor is uniformly doped,

$$C^2 = \frac{A^2 q N_D \epsilon_s}{2(V_{bi} - V - \frac{kT}{q})}$$

or

$$\frac{1}{C^2} = \frac{2(V_{bi} - V - kT/q)}{A^2 q N_D \epsilon_s} \qquad (3.26)$$

where A is the area of the contact between the metal and semiconductor and N_D is the donor density in the semiconductor By extrapolating $1/C^2$ vs. V plot to $1/C^2 = 0$, as shown in Figure 3.9, we obtain

$$V = (V_{bi} - \frac{kT}{q}) = V_i \qquad (3.27)$$

where V_i is the voltage intercept.

The barrier height can then be obtained from

$$\phi_{Bn} = V_i + V_n + kT/q - \partial\phi \qquad (3.28)$$

where V_n is the depth of the Fermi level below the conduction band which can be calculated if the doping density is known, and $\partial\phi$ is the image force barrier

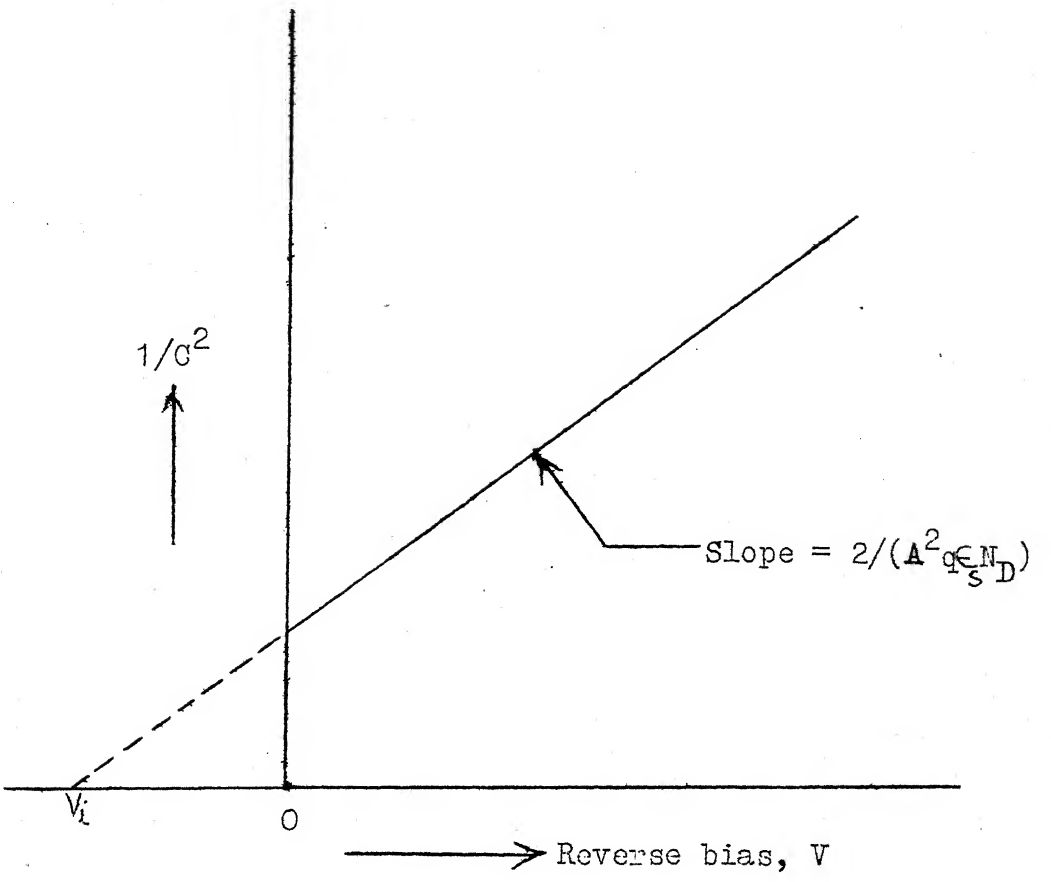


Figure 3.9: Capacitance-voltage characteristics of metal-semiconductor contact.

lowering. The correction term kT/q results from the contribution of the majority carriers[5].

Also the slope of the curve shown in Figure 3.9 can be used to determine the doping density N_D by using the equation

$$N_D = \frac{2}{q \epsilon_s} \left(- \frac{dV}{d(1/C^2)} \right) \qquad (3.29)$$

3.5.3 Photoelectric Measurement:

Photoelectric method is the most accurate, direct and probably the most reliable method of determining the barrier height. When a monochromatic light is incident upon a metal surface, photocurrent may be generated if the conditions mentioned below are satisfied. The set up is shown in Figure 3.10(a). For illumination from the metal side if the metal is not too thick and if $h\nu > q \phi_{Bn}$, the light can generate excited electrons in the metal. If the film is thin enough and $h\nu > E_g$, the light can also generate electron-hole pairs in the semiconductor. These are shown in Figure 3.10(b).

A typical photoresponse curve from a metal-semiconductor contact is shown in Figure 3.10(c). The dependence of the photocurrent on photoenergy for $(h\nu - q \phi_{Bn}) > 3$ kT is given by[10]

$$\sqrt{J_{photo}} = K(h\nu - q\phi_{Bn}) \qquad (3.30)$$

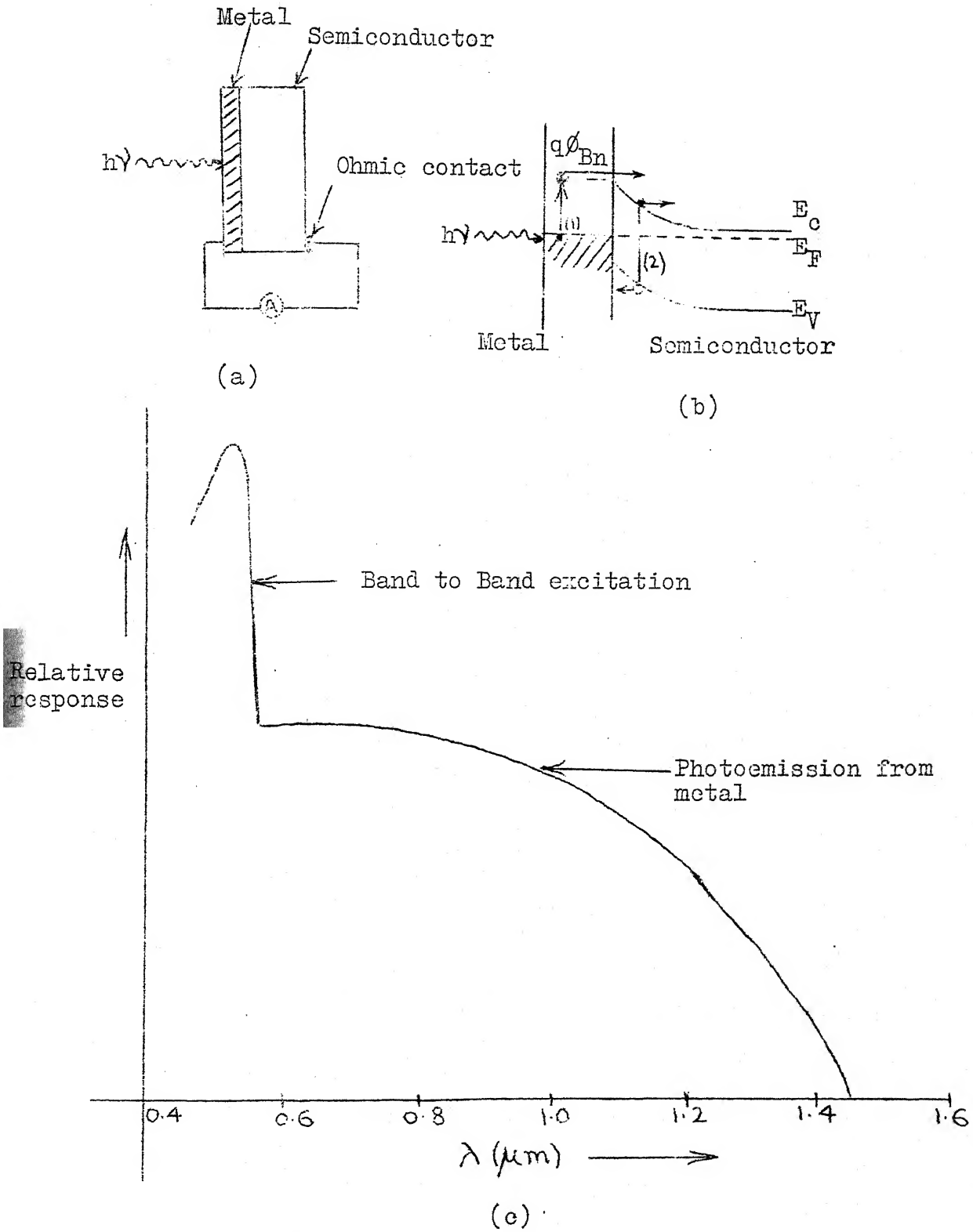


Figure 3.10: (a) Schematic setup for photoelectric measurement

(b) Energy band diagram for photoexcitation process.

(c) Relative photoresponse as a function of photo wave length.

where K is a constant of proportionality. This equation shows that a plot of $\sqrt{J_{photo}}$ vs. $h\nu$ is a straight line which when extrapolated gives an intercept ϕ_{Bn} on $h\nu$ axis.

The photoresponse method can also be used to determine the image force dielectric constant ϵ_d since we know[11]

$$\partial\phi = \left[\frac{q^3 N_D (V+V_i - \frac{kT}{q})}{8\pi^2 \epsilon_s \epsilon_d^2} \right]^{1/4} \qquad (3.31)$$

Thus if the barrier height is measured as a function of applied reverse bias, $\partial\phi$ can be determined and a plot of $\partial\phi$ vs. $(V + V_i - kT/q)^{1/4}$ gives a straight line whose slope can be used to determine the value of ϵ_d.

A few comments regarding these methods of measurement may not be out of place. Equation (3.26) has been derived based on the assumption that the doping of the semiconductor is uniform. If the doping of the semiconductor is not uniform, the C-V method would, however, not be reliable. The non-uniform doping of the semiconductor also affects the current-transport mechanizm and hence the I-V characteristics of the Schottky barriers, thus making measurement of barrier height unreliable.

The photoelectric method is, as mentioned earlier, the most direct method. No assumptions are made in this method except those mentioned above. The only constraints

that could be put on this method are that the thickness of the metal that is evaporated on the semiconductor should be small enough so that the photoemission is made possible, and the absorption of the incident photons by the metal film varies slowly with the photon energy.

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Chapter 4

OHMIC CONTACTS TO GALLIUM ARSENIDE

Ohmic contacts play an important role in the operation of semiconductor devices. These electrical contacts which are made by means of metallic conductors to the semiconductor crystals should exhibit lowest possible series resistance so that the efficient and reliable operation of the devices, particularly of microwave GaAs devices, is ensured.

Ideally, an ohmic contact should depict a current voltage relationship obeying ohm's law. This means that (1) the threshold voltage for the zero current should be small, and (2) the voltage to current ratio should remain constant, within the ranges of interest, with the applied voltage. These two requirements should hold say from about a millivolt to several volts.

The characteristics of a good ohmic contact are: (1) the contact should not be patchy if it is to have a low resistance; (2) it should allow the carriers to pass across the transition region without any modifications into them, that is, it should not inject carriers into the device or hinder the motion of carriers at the transition region; (3) the resistance and the properties of the contact should not change with time and ambient and should

be stable at different temperatures, and (4) the contact should be mechanically strong to support the device and should be as noise free as possible.

The general requirements for obtaining ohmic contacts are as follows:

(1) The desirability of a low potential barrier between the metal and semiconductor which under ideal conditions should be zero.

(2) The need to avoid high resistivity intervening compounds between the metal and semiconductor.

(3) The need to suppress the carrier injection from the metal into the semiconductor.

(4) The advisability of a heavy doped layer in the semiconductor region just under the metal.

Various methods[1] have been used to make ohmic contacts to GaAs. Alloying of tin[2] spheres in vacuum at temperatures between 300 - 450°C has been used. This method provides poor wetting and contacts are not always symmetrical. Tin-Nickle[2] have been used to provide better contacts.

A series of experiments were conducted by Matino and Tukumagee[4] to investigate the contact resistance of a number of metals (Ag, Au, Mo, Cr, Ti) and alloys such as Sn-Ag, In-Ag, Sn-Ge-Ag, Ge-Au, Ag and In-Ge-Ag on both n and p-types GaAs in a wide resistivity range. The

contact resistance was found to be highly dependent on the carrier concentration of GaAs. Whereas Mo-Cr contacts were ohmic on p-type GaAs, good ohmic contact on n-type material were obtained by Ag-In-Ge and Ag-Sn-Ge and In-Ag alloys provided the carrier concentration was not less than $10^{18}/cm^3$. For lower carrier concentrations appreciable contact resistance was observed.

Swartz and Sarace[5] have tried a large number of fluxes to clean the GaAs surface and promote better wetting. They have found that though most of the Iodine fluxes show a very poor performance, Chlorine and Bromine fluxes of Pb and Sn when used with small spheres of these metals gave good contacts on n-type GaAs of as low carrier concentration as $10^{16}/cm^3$.

Ge-Au, eutectic with 88 percent Au and 12 percent Ge, and Ni as wetting agent, have been used by Gunn[6] to make good ohmic contacts to n-type GaAs in wide resistivity range. Contact resistance on high resistivity material was, however, quite high.

More recently In-Au and Sn-Au have been used to obtain excellent ohmic contacts to n-GaAs of resistivity ranging from $1x10^{-3}$ to 1500 ohm-cm. and also on epitaxial grown layer[7].

4.1 EXPERIMENTAL WORK

In the present work we have used the technique developed by Paola[7] to make ohmic contact to n-GaAs. The details are described below:

4.1.1 Specifications of Starting Material and Surface Preparation:

The wafers used in the present work were n-type GaAs. Single crystals as grown (not intentionally doped) ingot of n-type GaAs having (111) orientation and a bulk resistivity of 18×10^{-3} ohm-cm (see Section 4.1.5) was cut into 1 mm. thick circular slices with the help of a wire saw. These wafers were lapped in succession with 9 microns, 5 microns and 1 micron Alumina powder to obtain the desired thickness.

An alternate and less time consuming method developed by the Electrical Engineering Department of Carnegie Mellon University, Pittsburg, U.S.A. was also tried though most of the devices were fabricated by the method described above. In this new method the wafers were lapped with 9 microns (if necessary) and 5 microns Alumina powder, respectively. Then the wafers were rubbed in the figure of eight on polish felt or ordinary silk cloth supported by glass-plate using a solution consisting of 20 parts of distilled water, 1 part of chlorax (5 percent solution of NaClO) and 1 part of Breec shampoo till scratch free mirror looking surfaces were obtained.

The lapped wafers were subjected to the following cleaning procedure:

The slice was first cleaned ultrasonically in distilled water for two minutes. It was then cleaned for five minutes in boiling trichloroethylene, for ten minutes in boiling accetone and was storcd in methanol. After this the slice was polished in 5 percent solution of Bromine in methanol[8] at room temperature using hand stirring. During the polishing operation both surfaces of the wafer were exposed to the etchant for equal amount of time and etching was continued till a smooth looking surface was obtained. The etchant was removed by successive dilutions and the slice was boiled for 2 minutes in distilled water. This was followed by a 5 minute boiling in Methanol. Finally, the hot methanol was replaced by the cold methanol in which the sample was stored till further processing. During cleaning and etching operationssolution changes were made as rapidly as possible to minimize the surface contamina-tions.

Since side A and side B of gallium arsenide are made up of gallium and arsenic atoms, respectively, these two sides get etched differently. Side A has many clearly defined etch pits whileas side B has no pits of this type. Ohmic contacts have been fabricated on side A and Schottky barriers have been fabricated on side B of these chemically prepared wafers.

4.1.2 Fabrication technology of Ohmic Contacts:

Before the diodes were fabricated, ohmic contacts to GaAs were made by evaporating an In-Au composition (90:10 by weight) into the specimen at a pressure of about $5x10^{-6}$ torr and by subsequent alloying of the evaporated layer (thickness 2500^{o}A measured with the help of Unitron microscope, see Appendix B) with GaAs at a temperature of 550^{o}C for about 30 seconds in an inert atmosphere. The evaporation of the contact metal was performed in an oil diffusion pump vacuum system. The bell jar was always kept under vacuum except for very short periods when it (bell jar) had to be removed in order to load the wafer in this system. Once the wafer was placed inside, the bell jar was quickly lowered. The total time consumed from the moment the bell jar rises off the face-plate to the time it returns following the placement of the wafer was on an average twenty seconds. Immediately after loading the wafer the pump down was started and when the pressure reached approximately $5x10^{-6}$ torr, the evaporation was begun.

Before evaporation In-Au composition was cleaned in dilute Hcl, boiled in distilled water for two minutes and stored in methanol.

Evaporation was performed through copper-berrylium metal mask. The mask was cleaned before use in very dilute HNO_3, boiled in distilled water for about two minutes and stored in methanol.

A simple furnace and a quartz carrier, fitted with a quartz boat at a one end and the thermocouple tip right beneath the quartz boat, were used for the alloying purpose. The furnace was put on about 8-10 hours before use for temperature stabilization purpose. When the alloying was to be done, the wafer was loaded on the boat and the boat was pushed into the temperature stabilized furnace to the predetermined position where the temperature was 550°C. It was then removed to a cooler section of the furnace after thirty seconds and then allowed to cool naturally. The inert atmosphere was provided by passing nitrogen through the furnace at a constant rate of about 5 litres per minute. Non-corrodable Tefflon tubing was used to transport the nitrogen gas. The nitrogen gas supply was started about ten minutes before the actual alloying and was stopped only when the temperature of the wafer cooled down to about 100°C after alloying.

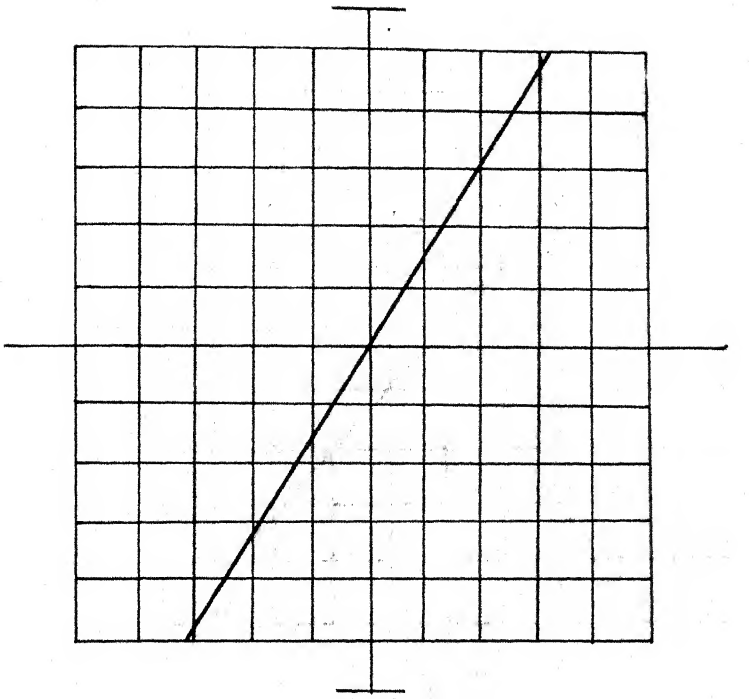
4.1.3 Evaluation of Ohmic Contacts:

The contacts were evaluated by the following two methods:

1) V-I characteristics
2) Potential-distance profile.

4.1.3.1 V-I Characteristics:

The contacts were examined for linearity on a Tektronix Curve Tracer. Figure 4.1(a), (b), (c) and (d) shows the V-I characteristics between two dots. In all



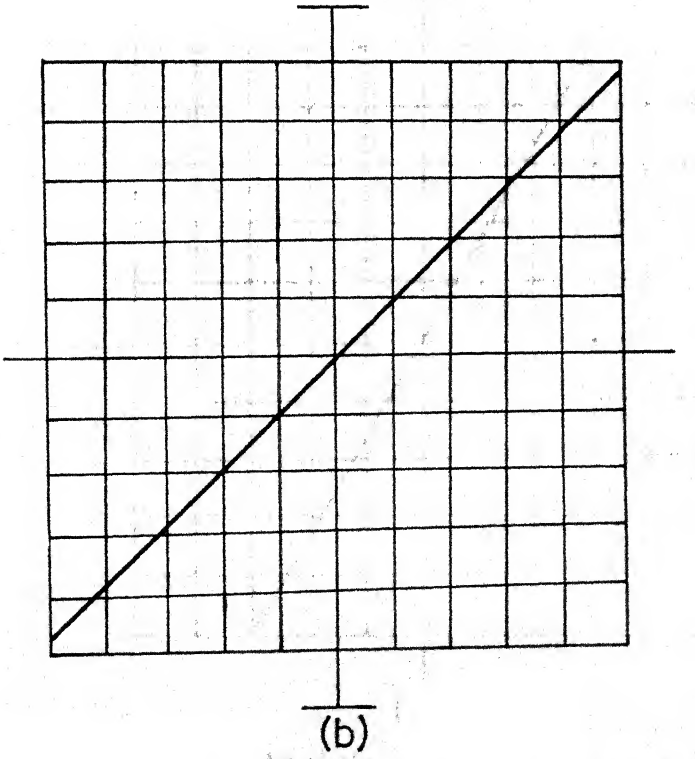
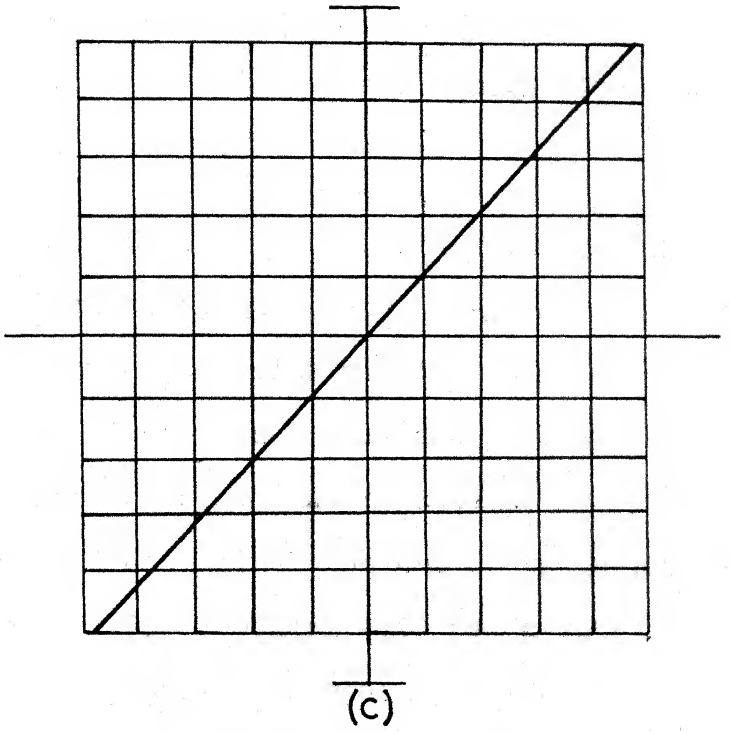


Fig. 4.1 I-V characteristics of ohmic contacts on GaAs at 300 °K
(a) 5 mA/Div. Vert., 0.01 Volt/Div. hor.
(b) 20 mA/Div. Vert., 0.01 Volt/Div. hor.



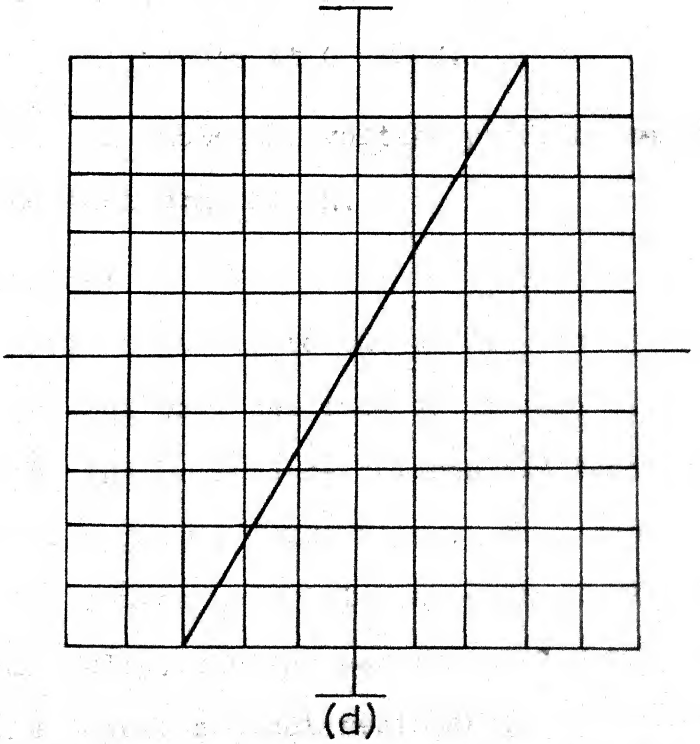


Fig. 4.1 I-V characteristics of ohmic contacts on GaAs at 300°K
(c) 20 mA/Div. Vert., 0.02 V/Div. hor
(d) 5 mA/Div. Vert., 0.01 V/Div. hor

the cases shown the resistance between contacts at 300°K is about 1-1.2 ohms which is quite high as compared to the spreading resistance of 0.15 ohms.

4.1.3.2 Contact Evaluation by Potential Profile Studies:

Contact resistances and non-linearities can be investigated by a potential profile method. Several In-Au contacts were alloyed in a line and at equal distances across the surface of a GaAs crystal as shown in Figure 4.2. Current was passed through the end contacts and voltage was measured with a D.C. Boonton Meter as a function of dot position. The profile was measured first in position 1 and then in position 2. Ohmic contacts should produce a straight line with the intercepts at 0 and V.

Figure 4.2 shows the voltage profile measurement curves for contact evaluation.

4.1.4 Discussion:

The ohmic contacts to the diodes having very low contact resistance were obtained after many trials. In early attempts the resistance between two contact dots was about 30 ohms, a fairly large value. When cleaning of the sample and the source materials was emphasized, and alloying done more carefully, the contact resistance was considerably reduced. The lowest contact resistance that was obtained was about one ohm. The I-V characteristics were seen to be linear upto about 20 volts and the contact properties were quite stable.

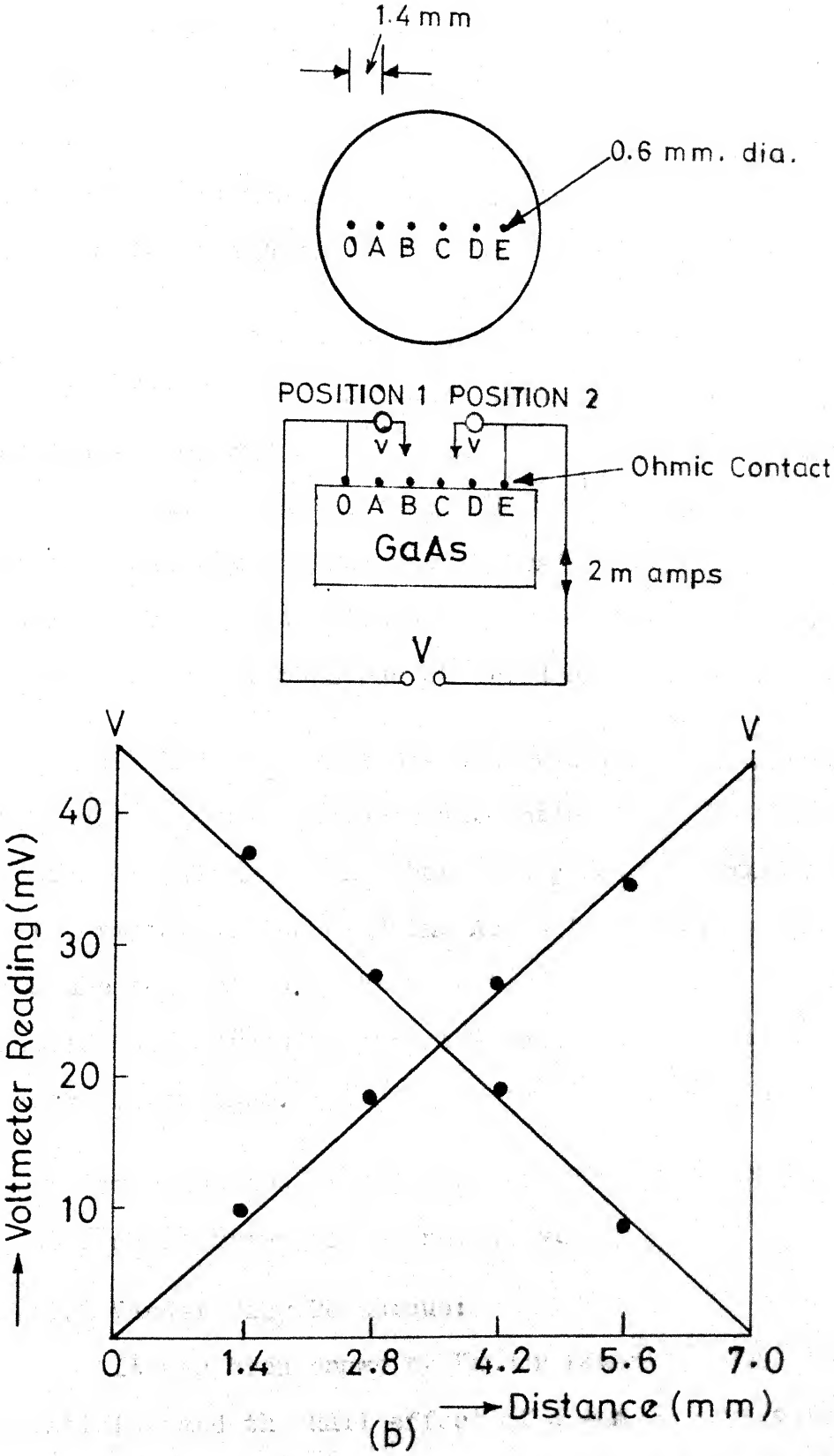


Fig. 4.2 Observed potential profile of six ohmic contacts on n-GaAs

Voltage profile measurements as depicted in Figure 4.2 show that the voltage drops were nearly uniform with distance. The straight line was seen roughly passing through the origin of the curve. Thus, the contact resistance was negligible as compared to the bulk resistance.

Paola[7] had concluded that an optimum thickness of 2300 A^{o} with 90:10 In-Au composition gave good ohmic contacts with low resistance. This was also verified in the present work. When the thickness of the evaporated layer was considerably smaller than 2300A^{o} or much larger than 2300A^{o}, the contact resistance was not as low as one would expect. However, this was observed only qualitatively.

Another fact that was observed was that the wafers on which the ohmic contacts were made became brittle. The possible explanation that has been given by Poala is that an intermetallic compound In_2 Au is formed which tends to make the contact quite brittle. The wafers had to be handled more carefully once the ohmic contacts were fabricated on them.

4.1.5 Determination of the Resistiviy and the Carrier Concentration of the n-GaAs wafers:

5.1.5.1 Vander Pauw Technique:

It has been shown by Vander Pauw[9] that the specific resistivity and the Hall effect of a sample of arbitrary shape can be measured without knowing the current pattern if the following conditions are fulfilled:

(1) The contacts are at the circumference of the samplee.

(2) The contacts are sufficiently small.

(3) The sample is homogeneous in thickness

(4) The surfacex of the sample is singly connected, i.e., the sample does not have isolated holes.

For a thin sample of arbitrary periphery Vander Pauw proved that the resistivity is given by

$$\rho = \frac{\pi t}{\ln 2}\left(\frac{R_{AB,CD} + R_{BC,DA}}{2}\right) + f\left(\frac{R_{AB,CD}}{R_{BC,DA}}\right) \text{ ohm-cms} \qquad (4.1)$$

where

t = thickness of the sample in cms.

$$R_{AB,CD} = \frac{V_D - V_C}{I_{AB}}$$

$$R_{BC,DA} = \frac{V_D - V_A}{I_{BC}}$$

and the function $f\left(\frac{R_{AB,CD}}{R_{BC,DA}}\right)$ is plotted in Figure 4.3.

When a magnetic field is applied perpendicularly to the sample, Hall mobility is given by

$$\mu_H = \frac{t}{B}\,\frac{\partial R_{BD,AC}}{\rho} \quad \text{cm}^2/\text{volt-sec.} \qquad (4.2)$$

where B is the magnetic induction (Wb/cm^2),

$$R_{BD,AC} = \frac{V_C - V_A}{I_{BD}}$$

and $\partial R_{BD,AC}$ is the change in the resistance $R_{BD,AC}$ due to application of the magnetic field.

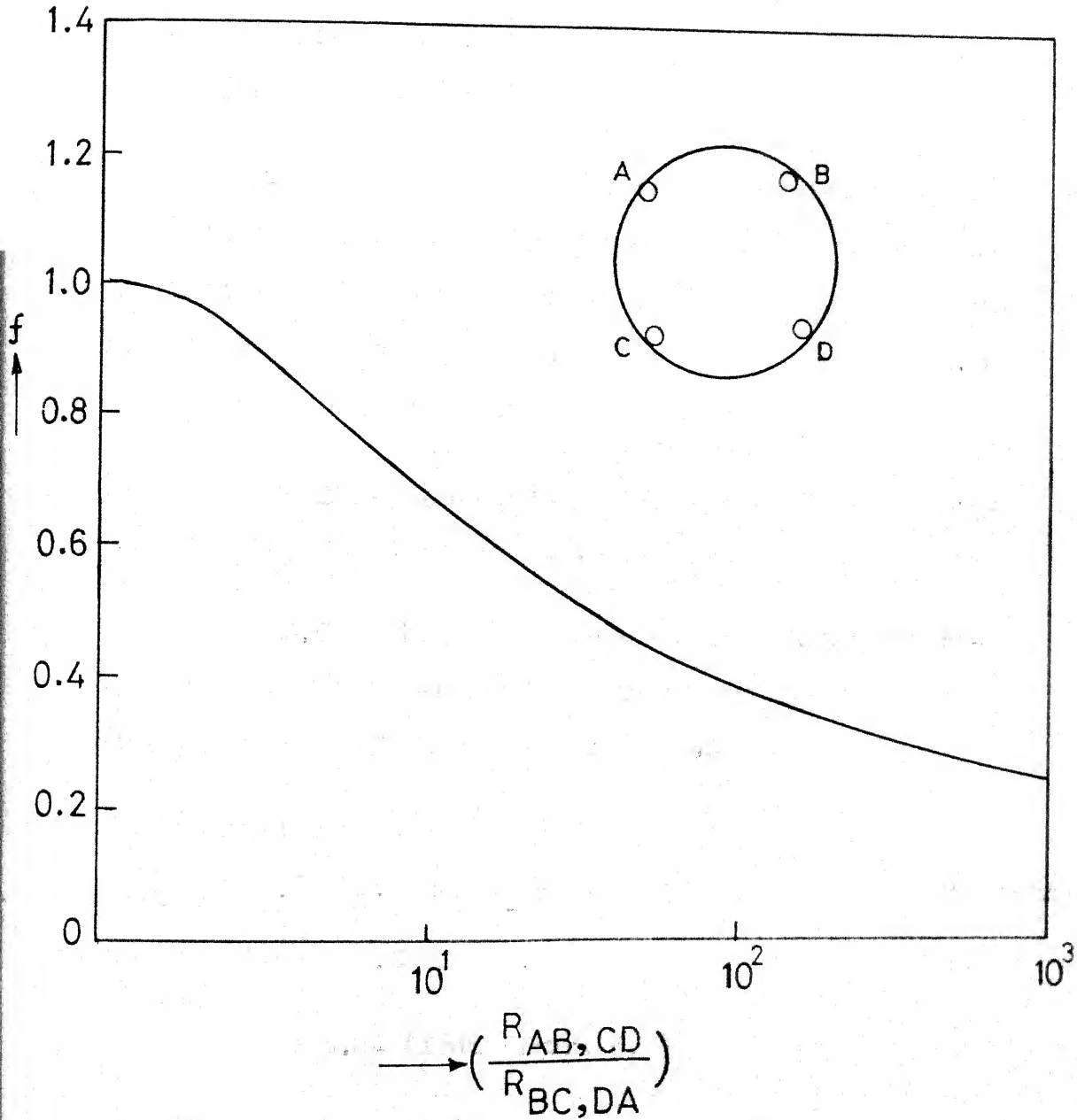


Fig. 4.3 Plot of f with the ratio $\left(\frac{R_{AB,CD}}{R_{BC,DA}}\right)$

In the presence of the magnetic field B,

$$B = 0.73 \times 10^{-5} \text{ Wb/cm}^2$$

$$R_{BD,AC} = 0.0225 \text{ ohms}$$

so that $\mu_H = 5200 \text{ cm}^2/\text{volt-sec.}$ (from equation 4.2)

and carrier concentration = 6.67×10^{16} per cm^3.

whereas effective density of states in the conduction band of GaAs is $4.7 \times 10^{17} \text{ cm}^{-3}$.

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Chapter 5

SCHOTTKY BARRIERS ON GALLIUM ARSENIDE

5.1 SAMPLE PREPARATION AND DIODE FABRICATION

The GaAs slice to which ohmic contact had already been made was etched for ten seconds in the 5 percent solution of Bromine in methanol[1] and was boiled in distilled water for two minutes. It was then stored in methanol. It was observed in some experimental runs that the side B on which the metal was to be evaporated for Schottky barrier contact got contaminated during the alloying of ohmic contacts. This contamination resulted in the formation of an insulating layer on the GaAs surface when this was the case. Side B was then lapped very carefully with 5 and 1 micron Alumina powder. The wafer was then cleaned ultrasonically in distilled water for two minutes, solvent cleaned and then etched in a 5 percent solution of Bromine in methanol at room temperature using hand stirring. The etchant was then removed in the same way as has already been discussed in Chapter 4, and the wafer was then stored in methanol. While the side B of the wafer was etched, side A having ohmic contact was covered with black wax. This wax was later removed with the successive flushing of the wafer in trichloroethylene. After this the wafer was again boiled in trichloroethylene for 5 minutes to remove any possible impurities, in accetone for 10 minutes to remove

trichloroethylene and then stored in methanol. The wafer was then removed from methanol for use, carefully dried and after this, was transferred to the vacuum system. Schottky barriers were fabricated by vacuum evaporation of Indium on this wafer through metal masks. Indium (99.99 percent purity) was obtained in the form of dots. Evaporations were performed in the oil diffusion pump vacuum system at a pressure of better than $1x10^{-6}$ torr. Tungesten boat was used for the evaporations and was cleaned and pre-outgassed before use in vacuum at temperatures higher than that at which the vaporations were performed. Clean Copper-Berrylium masks were used to define the diode geometry and contact area. In all experiments circular areas with diameters ranging from 1.5 to 4 mm were used. Various film thicknesses were used which were measured after evaporation with the help of unitron microscope. A standard thickness of $1000A^{o}$ was used for most of the work. Control of the duration of evaporation was achieved by using a shutter between the boat and the GaAs wafer.

Electrical connections were made to the semiconductor and the metal layers by pressing gold wire tip having molten Indium on it as described earlier in Chapter 4. The device was then mounted on a clean glass slide.

5.2 MEASUREMENT OF BARRIER HEIGHT

The following methods were used to measure the barrier height of the In-GaAs Schottky barriers:

(i) I-V characteristics,

(ii) C-V measurement, and

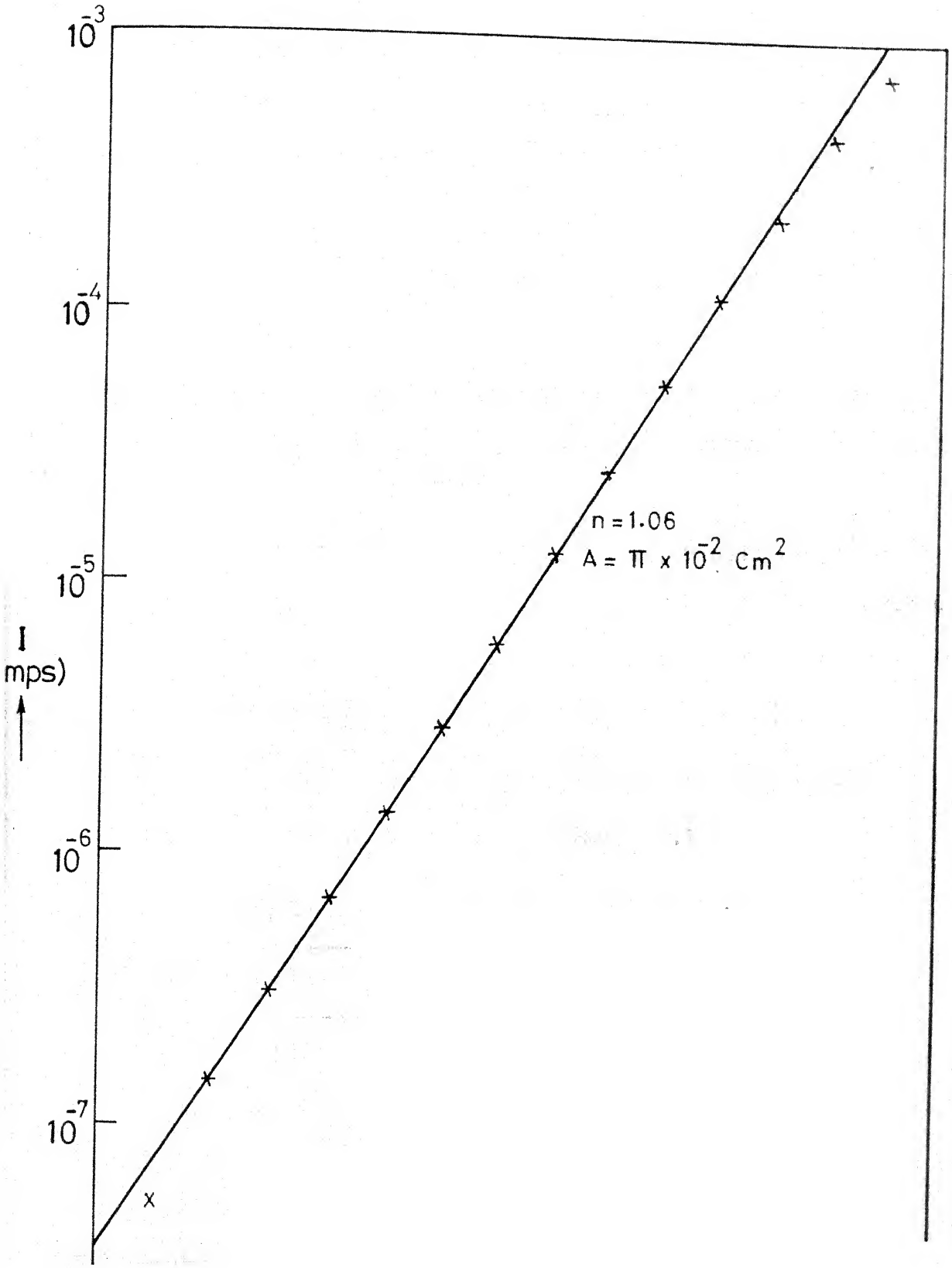
(iii) photoelectric measurement.

5.2.1 I-V Characteristics:

The first measurement carried out on the fabricated In-GaAs Schottky barriers was the measurement of I-V characteristics. This measurement was performed with the help of H.P. Model 412A D.C. VTVM as Voltmeter, Boonton Sensitive DC Meter Model 95A as ammeter and H.P. Power Supply Model 6026A as variable voltage D.C. source. The device was fitted in a black box to avoid the external light falling on the metal surface as it was observed that the current shown by the ammeter changed in magnitude once the path of light rays was cut if the device was kept in the open. Figure 5.1 shows the lnI vs. V curve for a typical diode. From the slope of the curve in Figure 5.1 the value of n was obtained using the equation (3.22)

$$n = \frac{q}{kT} \frac{\partial V}{\partial (\ln J)} \qquad (3.22)$$

$= 1.06$ at $T = 300^{\circ}K$ for the diode characteristics shown in Figure 5.1.


10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
I
mps)
n = 1.06
A = π x 10^{-2} Cm^2

The extrapolated value of the current density to zero voltage gave the saturation current density J_s and the barrier height was calculated using the equation (3.24), namely

$$\phi_{Bn} = \frac{kT}{q} \ln\left(\frac{A^* T^2}{J_s}\right) \qquad (3.24)$$

$$q\phi_{Bn} = 0.76 \text{ eV}$$

for the Schottky barrier whose characteristics are shown in Figure 5.1. The value of the effective Richardson's constant A^* used was 120 amps/cm^2/K^{o2}.

The measured I-V characteristics for well prepared samples were near ideal obeying a relation which is described by

$$I = I_s(e^{qV/nkT} - 1)$$

where n varied from 1.06 to 1.1. Values of n and J_s for various good diodes are listed in Table 5.1.

TABLE 5.1: I-V CHARACTERISTICS AT 300^{o}K

Diodes	A, cm^2	n	I_s, amps	$q\phi_{Bn}$, eV
D_1	$\pi \times 10^{-2}$	1.10	8.2×10^{-8}	0.76
D_2	1.77×10^{-2}	1.09	2×10^{-8}	0.79
D_3	$\pi \times 10^{-2}$	1.06	3.5×10^{-8}	0.78
D_4	1.77×10^{-2}	1.10	5×10^{-8}	0.77
D_5	9.6×10^{-2}	1.08	5×10^{-7}	0.78

5.2.2 C-V Measurements:

The C-V measurements on various fabricated In-GaAs Schottky barriers were performed using a Boonton capacitance Bridge Model 74C-518. The bridge had a variable voltage in-built d-c supply on which was superimposed a 10 mV a.c. signal at a frequency of 100 KHz. Prior to its use, the bridge was tested for its accuracy by a standard capacitor. The H.P. Model 412A D.C. VTVM was used to measure the voltage applied across the diode terminals.

Plots of capacitance vs. reverse bias generally gave good straight lines which when extrapolated to the horizontal axis gave the voltage intercept V_i. Then using the equation (3.28), ϕ_{Bn} was calculated.

$$\phi_{Bn} = V_i + V_n + \frac{kT}{q} - \partial\phi \qquad (3.28)$$

V_n, the difference between the Fermi level and the conduction band can be calculated from the equation (5.1), i.e.,

$$n = N_c\, e^{\frac{-(E_c - E_F)}{kT}} = N_c\, e^{\frac{-qV_n}{kT}} \qquad (5.1)$$

where N_c is the effective density of surface states in the conductor band and is 4.7×10^{17} per cm^3 for GaAs, E_c is the energy of the bottom of the conduction band and E_F is the energy at the Fermi level.

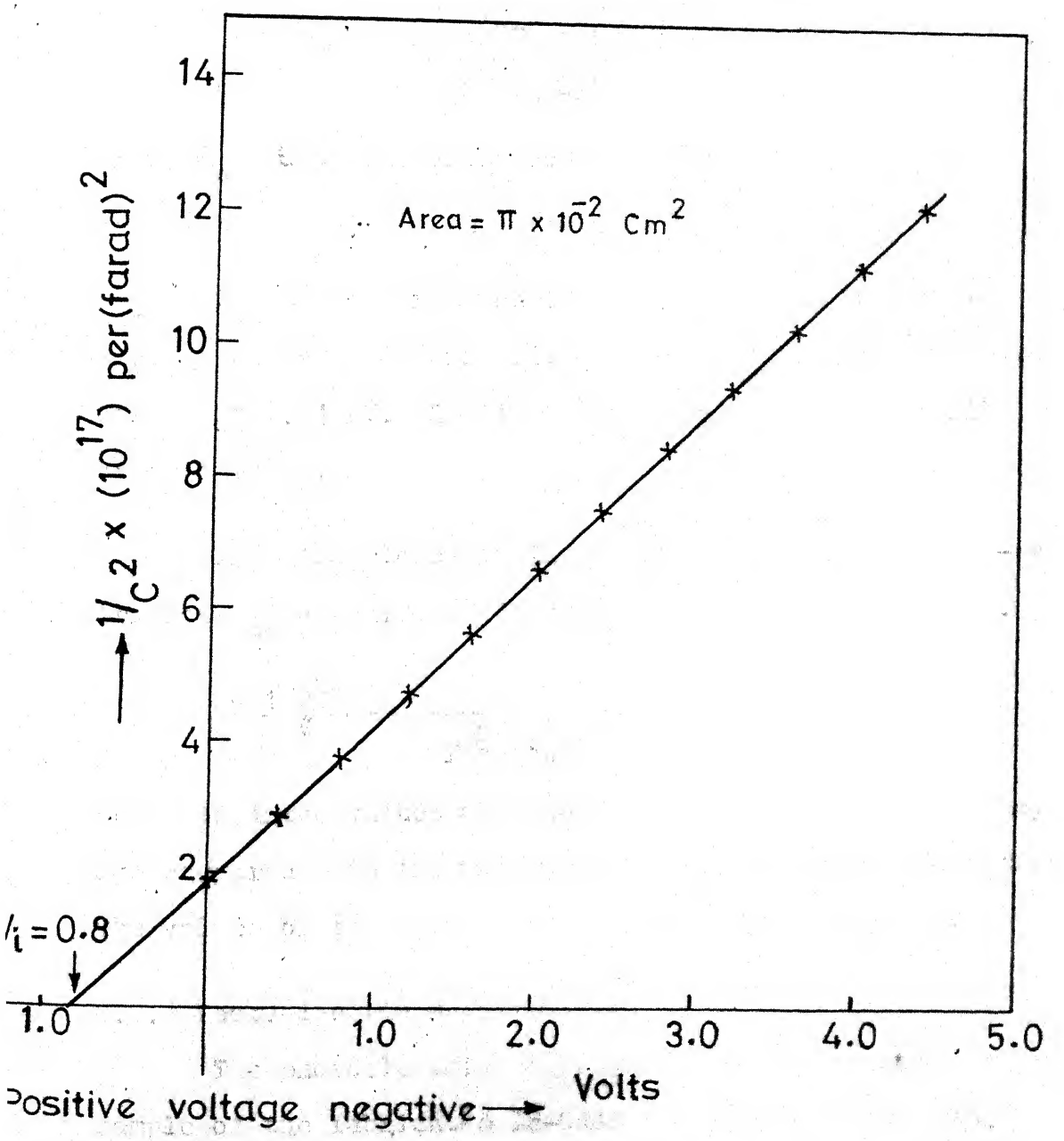


Fig. 5.2 Room temperature $1/C^2$ Vs V plot of In-GaAs schottky barrier diode

From the calculations using equation (5.1), we get

$$V_n = 0.05 \text{ volts}$$

$\partial\phi$ has been calculated using equation (3.31), i.e.,

$$\partial\phi = \left| \frac{q^3 N_D (V+V_i-\frac{kT}{q})}{8\pi^2 \epsilon_s \epsilon_d^2} \right|^{1/4} \qquad (3.31)$$

where $\epsilon_s = \epsilon_d$. Its value comes to about 35 mV at zero voltage.

V_i is read from the $1/C^2$ vs. V curve. A typical plot is shown in Figure 5.2, and the value of $q\phi_{Bn}$ obtained was about 0.84 eV. Similar plots were obtained for all other samples.

From the slopes of these curves the donor concentration N_D was calculated using the equation (3.29),ie.,

$$\frac{d(1/C^2)}{dV} = \frac{-2}{N_D \epsilon_o \epsilon_s A^2} \qquad (3.29)$$

The calculated values are tabulated in Table 5.2 where they are compared with the values obtained by Vander Pauw method. The values of the barrier height are also tabulated.

5.2.3 Photoelectric Measurement:

The photoelectric measurement was made on one sample of the fabricated In-GaAs Schottky barrier using a Gartner monocromater and an automobile headlight lamp (3 amps., 12 volts ratings). The photocurrent was measured by the Boonton Sensitive DC Meter. The zero bias photocurrent of this sample as a function of the wave length

TABLE 5.2: $1/C^2$ VS. V CHARACTERISTICS AT 300°K

Diodes	V_i, V	$q\phi_{Bn}$, eV	N_D	
			Resistivity measurements	Slope of $1/C^2$ vs.V curve
D_1	0.80	0.84	6.67×10^{16}	5.8×10^{16}
D_2	0.82	0.86	6.67×10^{16}	6.1×10^{16}
D_3	0.80	0.84	6.67×10^{16}	6.3×10^{16}
D_4	0.83	0.87	6.67×10^{16}	5.6×10^{16}
D_5	0.80	0.84	6.67×10^{16}	6.1×10^{16}

is shown in Figure 5.3. Figure 5.4 shows the variation of the photocurrent with the photon energy. Since we are interested in the photoemission part of the Figure 5.3 only this part of the curve is drawn in Figure 5.4. When this curve is extrapolated to the energy axis, the intercept on the photon energy axis directly gives the barrier height.

The value of ϕ_{Bn} determined from the photoresponse is shown in Table 5.3 where it is compared with the values obtained from I-V and C-V measurements.

The photoelectric measurement was also used to determine the image force barrier lowering that results with the application of the reverse bias. The photon energy was held constant and the photocurrent was measured

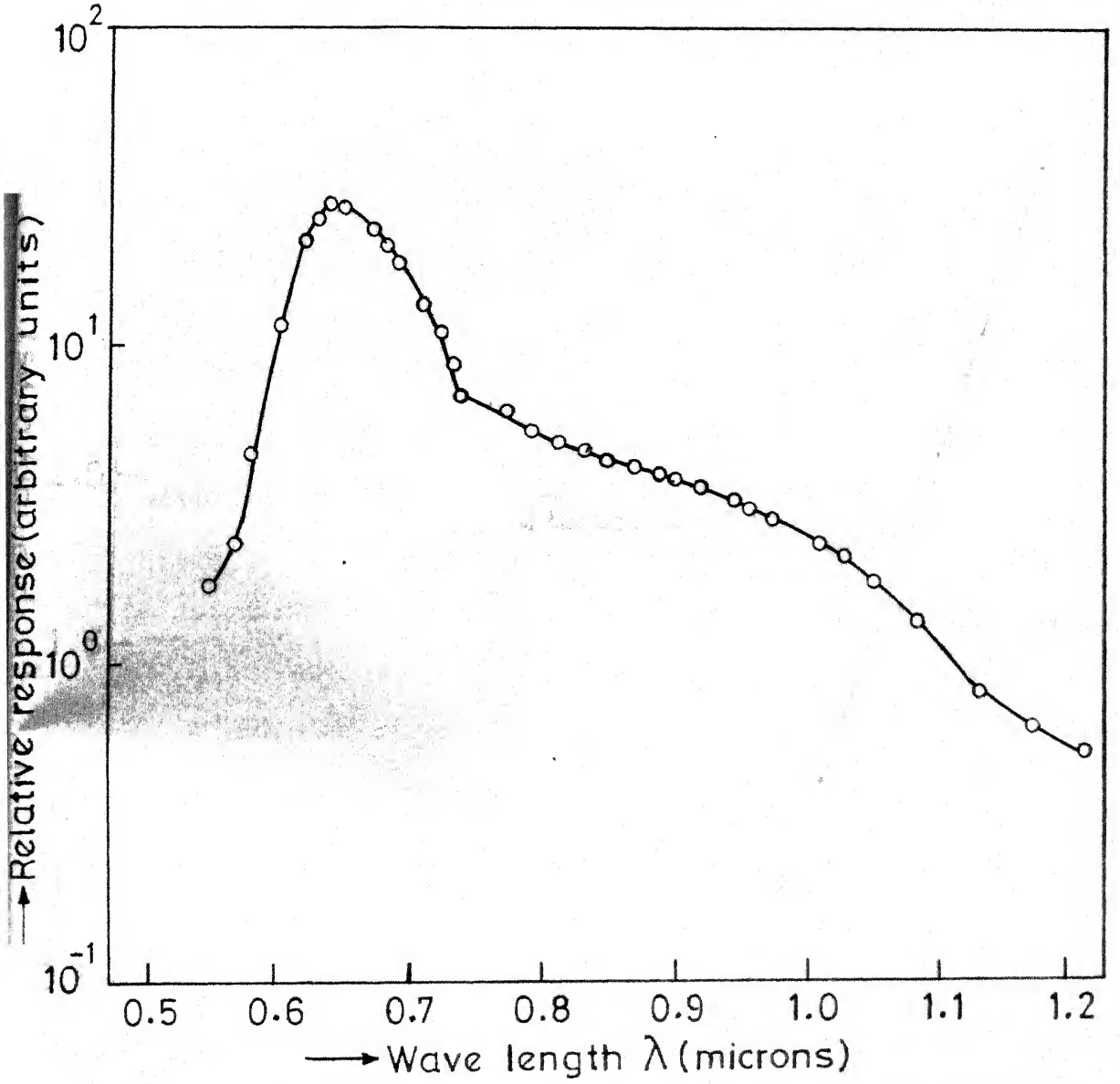


Fig. 5.3 Experimentally determined photo response Vs the wave length of the incident light given by an In-Ga As Schottky barrier contact

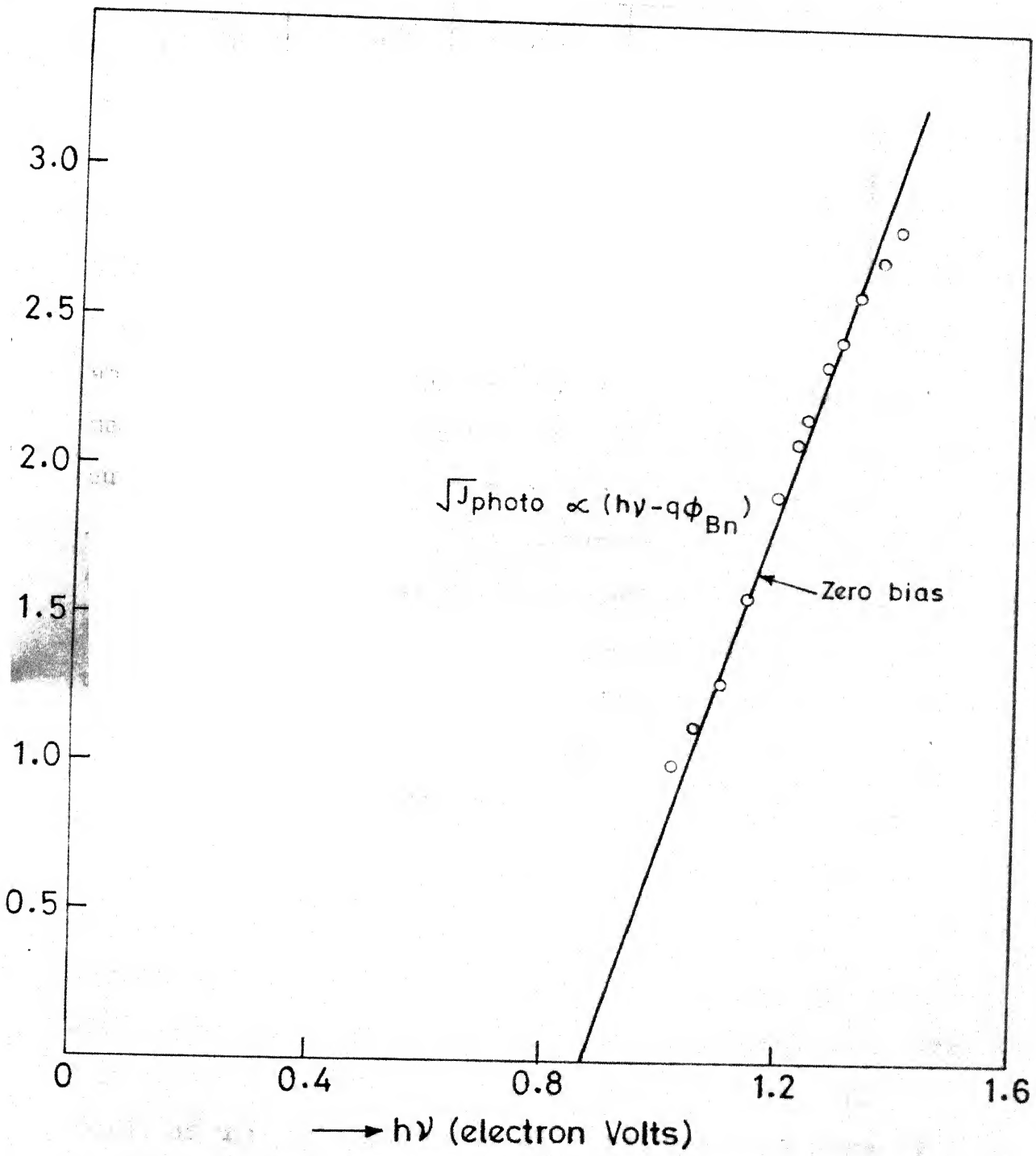


Fig.5.4 $\sqrt{\text{Photo response}}$ Vs photo energy

TABLE 5.3: COMPARISON OF BARRIER HEIGHTS IN eV

Diodes	I-V method	C-V method	Photoelectric method
D_1	0.76	0.84	-
D_2	0.79	0.86	-
D_3	0.77	0.84	-
D_4	0.77	0.87	-
D_5	0.78	0.84	0.87

as a function of the applied reverse bias. The ammeter measures the total current which includes the photoemission current and the leakage current because of the applied reverse bias. Since we were interested in the photoemission current only, the leakage was subtracted from the total current at each applied reverse bias. Then from the dependence of the photocurrent on the bias voltage the change in the barrier energy can be inferred using equation (3.30), namely,

$$\sqrt{J_{photo}} = K(h\nu - q\phi_{Bn}) \qquad (3.30)$$

provided that the proportionality constant K is not field dependent. The value of the barrier height, ϕ_{Bn}, at zero bias determined by photoelectric measurement was used in the calculation of $\partial\phi$, the lowering in barrier height. The result of this measurement is shown in Figure 5.5 where it is compared with the curve drawn using equation (3.31), namely,

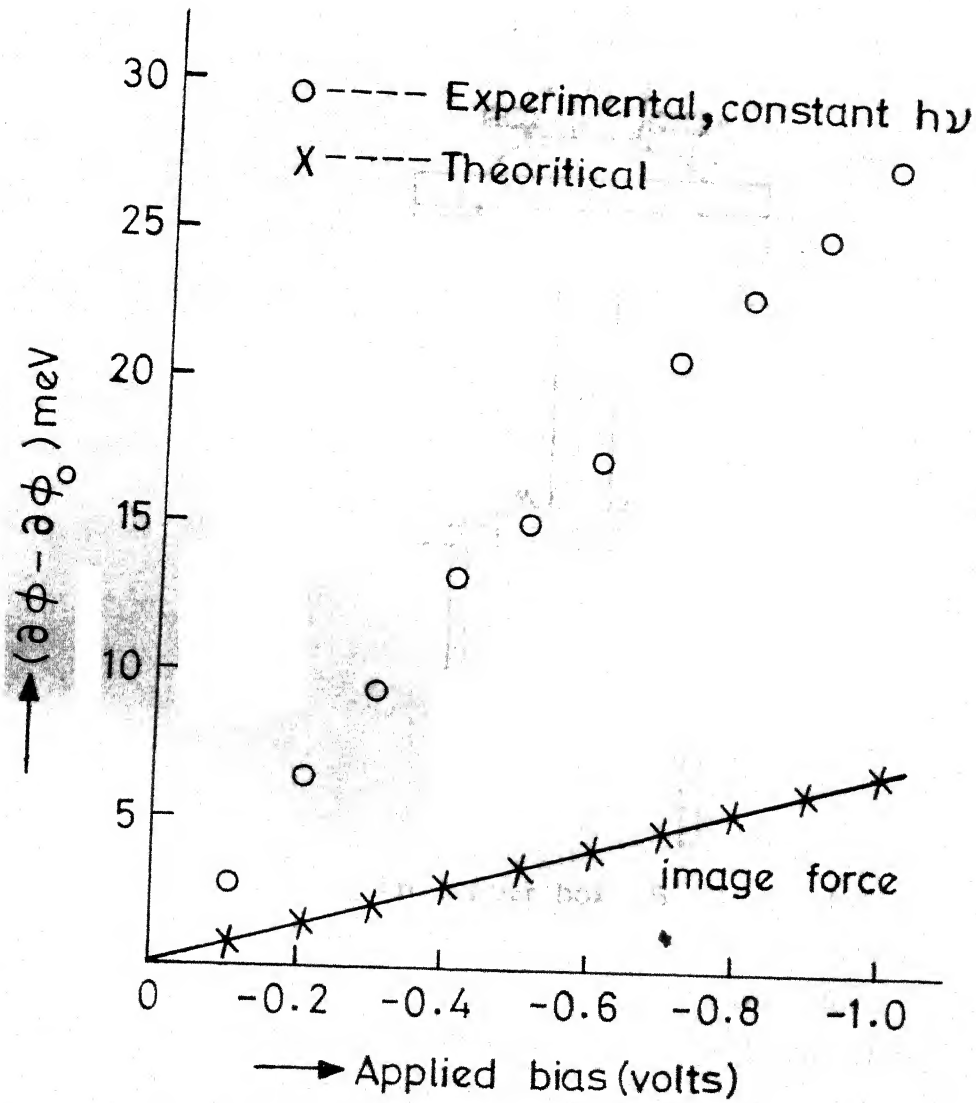
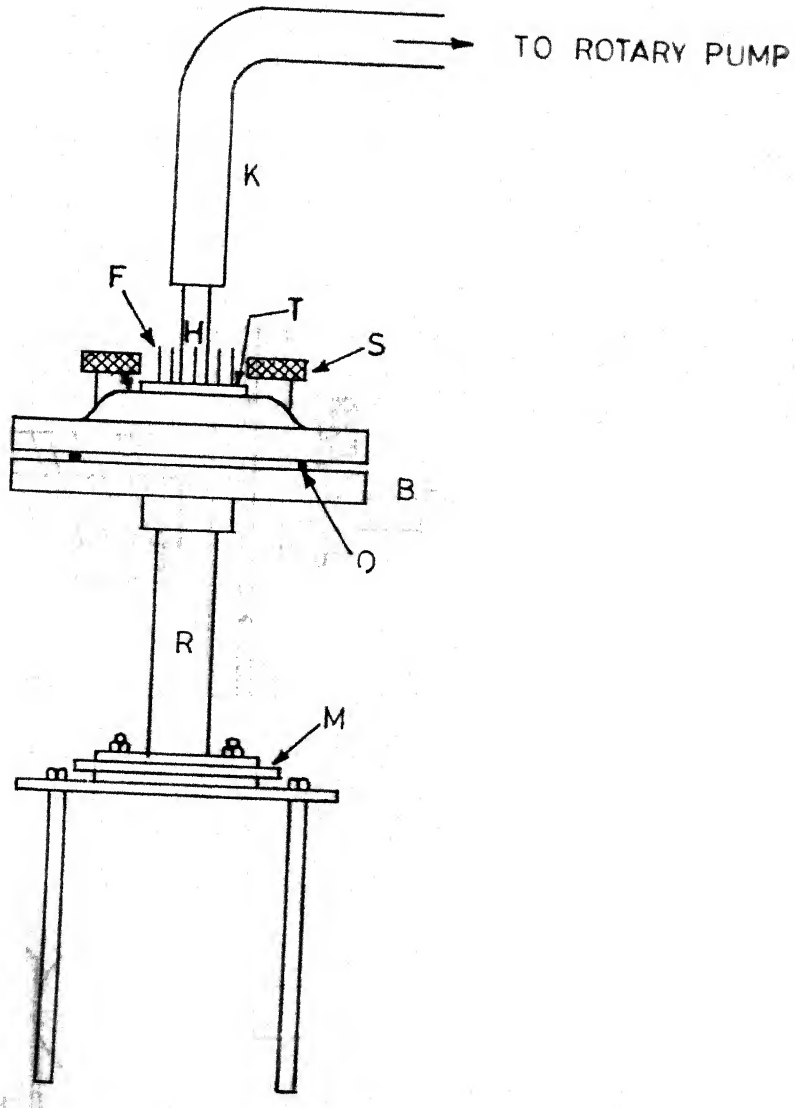


Fig. 5.5 Barrier lowering with the applied reverse bias



R	Rectangular copper box	B	Brass flange
O	Seat for o-ring	S	Brass screws
T	Teflon disc	F	Connectors
H	Stainless steel tube	K	Rubber tubing
M	Heater assembly		

Fig. 5.6 Apparatus for measurement of I-V characteristics of an In-GaAs Schottky barrier diode at and above 300 °K

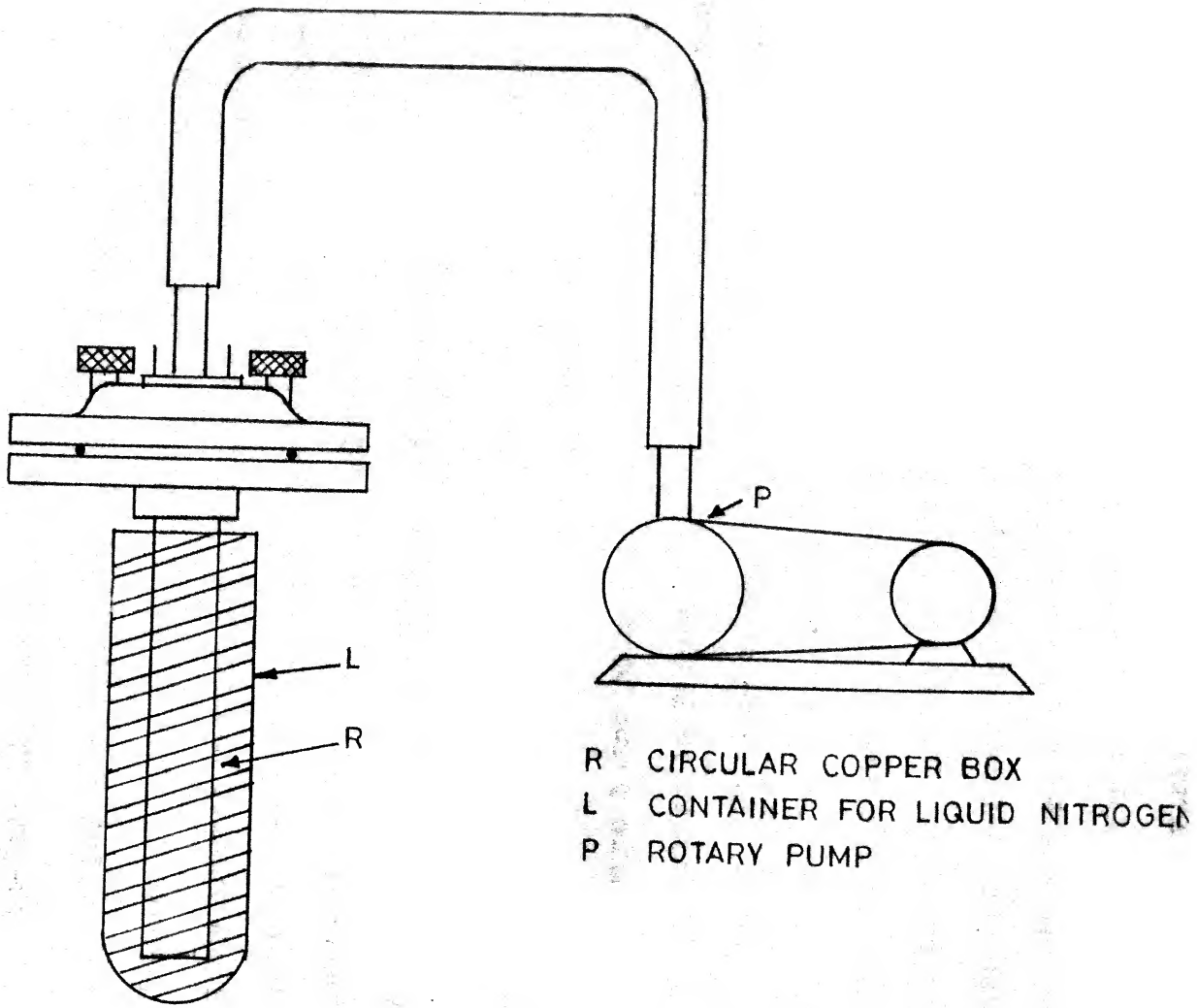


Fig.5.7 Apparatus for measuring the I-V characteristics of In-GaAs Schottky barrier at temperaturs below the room temperature

$$\partial\phi = \left[\frac{q^3 N_D (V+V_i - \frac{kT}{q})}{8\pi^2 \epsilon_s \epsilon_d^2}\right]^{1/4} \qquad (3.31)$$

where $\epsilon_s = \epsilon_d$ has been considered. In Figure 5.5, $\partial\phi_o$ is the barrier lowering at zero applied voltage.

5.3 TEMPERATURE DEPENDENCE OF I-V CHARACTERISTICS OF In-GaAs SCHOTTKY BARRIERS[3]

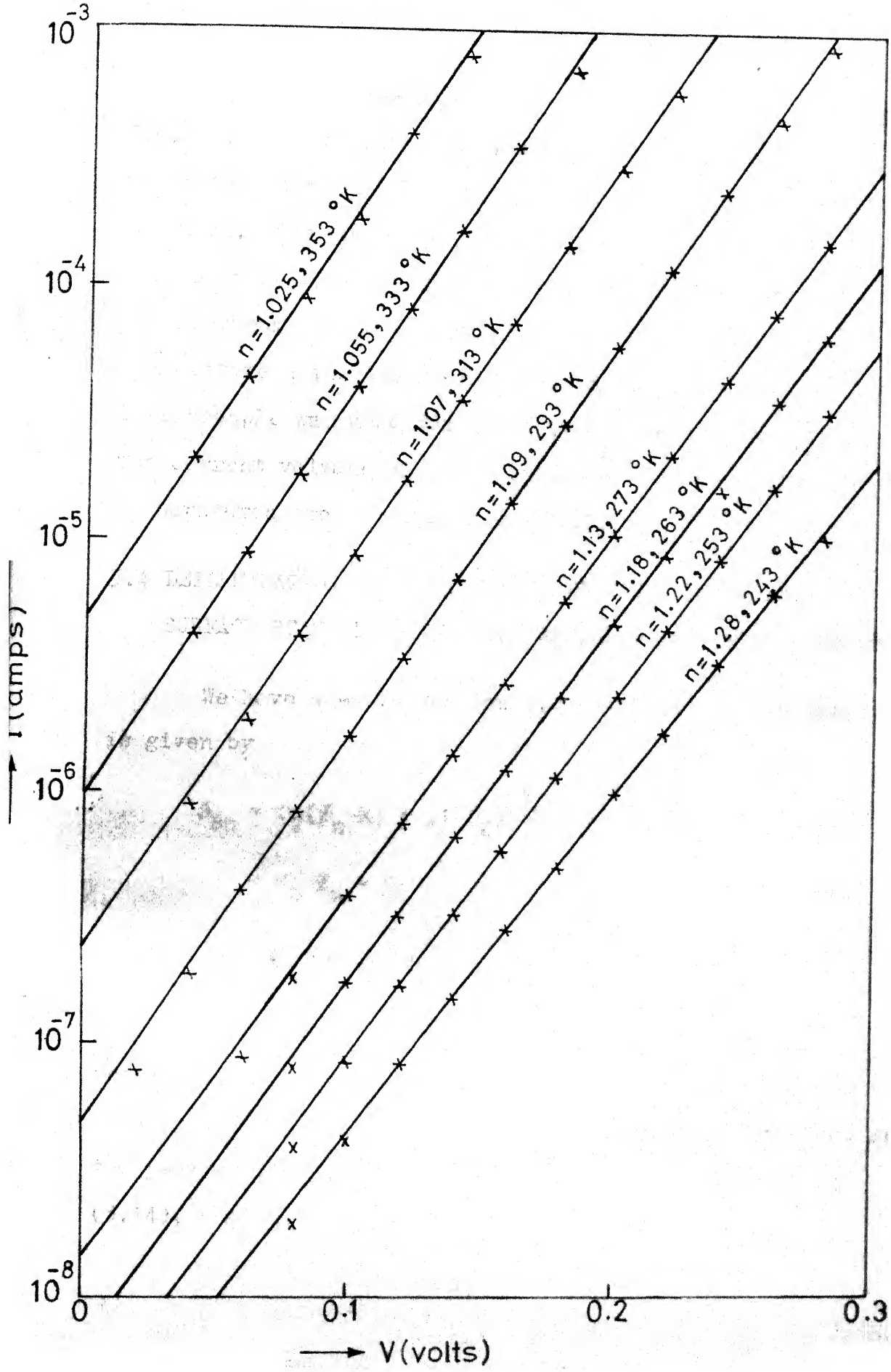
I-V characteristics of one of the fabricated In-GaAs Schottky barrier diodes was measured at various temperatures ranging from 243°K to 353°K. The measurements below the room temperature were made in vacuum in order to avoid the formation of water molecules on the fabricated device which would otherwise give wrong results.

The apparatus used for I-V measurements at room temperature and above is shown in Figure 5.6, and at temperature below room temperature is shown in Figure 5.7. The apparatus in Figure 5.6 consists of a rectangular pipe of copper (3" long) to which a copper sheet is soldered at the bottom and circular brass flange made at the top. The brass flange has an O-ring seat in it. The top cover of the brass flange has two holes in it, one for the stainless tube (welded for the purpose of creating vacuum) and the other for fixing tafflon disc. The tafflon disc has provisions for the vacuum seal connectors which are provided for making various electrical connections in order to make the measurements on the fabricated device placed inside the copper pipe.

The fabricated device mounted on the glass plate along with a copper-constantan thermocouple is placed in side the rectangular copper tube and all the terminals are soldered to the inside tips of the vacuum seal connectors. Copper wires are then soldered to the top tips of the connectors and these copper wires then go to the various instruments.

The copper rectangular containing the device is mounted on an nichrome-wire wound heater fixed on an asbestos sheet which is fixed on four copper rods. The temperature of the copper rectangular and hence of the device is controlled by controlling the supply voltage to the heater terminals by means of a variac.

The apparatus in Figure 5.7 for low temperature measurements consists of a circular pipe of copper about 7" long and 1.25" in diameter to which a copper sheet is soldered at the bottom and the circular brass flange made at the top. The brass flange has an O-ring for sealing purposes. Similar top brass flange is used here as has been used in the high temperature measurements. The vacuum in the pipe is created by Welch Duo seal rotary pump which is connected to the stainless steel tube by means of rubber tubing. Copper wires are again used to make the electrical and thermocouple connections using the similar technique as described above.


10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
I (amps)
0
0.1
0.2
0.3
V (volts)
n=1.025; 353 °K
n=1.055; 333 °K
n=1.07; 313 °K
n=1.09; 293 °K
n=1.13; 273 °K
n=1.18; 263 °K
n=1.22; 253 °K
n=1.28; 243 °K

The measurements were made using a H.P. Model 412A D.C. VTVM for voltage measurement, Boonton Sensitive D.C. Meter for measurement of current, and H.P. Power Supply was used. The thermocouple voltage was measured with the help of a sensitive Millivolt Potentiometer made by Leeds and Northrump Company, U.S.A., and was converted into temperature using the known data. A copper-constantan thermocouple was used for these temperature measurements. The current voltage characteristics obtained at different temperatures are shown in Figure 5.8.

5.4 DETERMINATION OF THE POSITION OF FERMI LEVEL AND SURFACE STATE DENSITY FROM BARRIER HEIGHT MEASUREMENTS

We have seen in Section 3.4 that the barrier height is given by

$$\phi_{Bn} = C_2(\phi_m - X) + (1-C_2)(\frac{E_g}{q} - \phi_o) - \partial\phi \qquad (3.12)$$

$$= C_2 \phi_m + C_3 \qquad (3.13)$$

where $C_2 = \epsilon_i/(\epsilon_i + q^2 \delta D_s)$

If we now draw a curve between ϕ_{Bn} and ϕ_m for various metals, we should get a straight line. The slope of this straight line will give the value of C_2 and the intercept on the y-axis will give the value of C_3. Using the equation (3.14), namely,

$$D_S = \frac{(1-C_2)\epsilon_i}{C_2\ \delta\ q^2}$$

$$\simeq 1.1 \times 10^{13}\ \frac{(1-C_2)}{C_2}\ , \quad \text{for}^4\ \delta = 4\ A^{\circ} \quad \text{and}\ \epsilon_i \simeq \epsilon_o \qquad (3.14)$$

We can calculate D_s, the density of surface states. Once D_s is known, the position of the Fermi level can be calculated using the equation (3.12),

$$\phi_o = \frac{E_g}{q} - (C_2 X + C_3 + \partial \phi)/(1-C_2) \qquad (3.12)$$

In the present work six metals, viz., In, Au, Al, Bi, Sb and Mg have been used. The fabrication of In-GaAs Schottky barriers has been described already in Section 5.1. The Schottky barriers on GaAs using Au, Al, Bi, Sb and Mg have been fabricated using the same technique as In-GaAs.

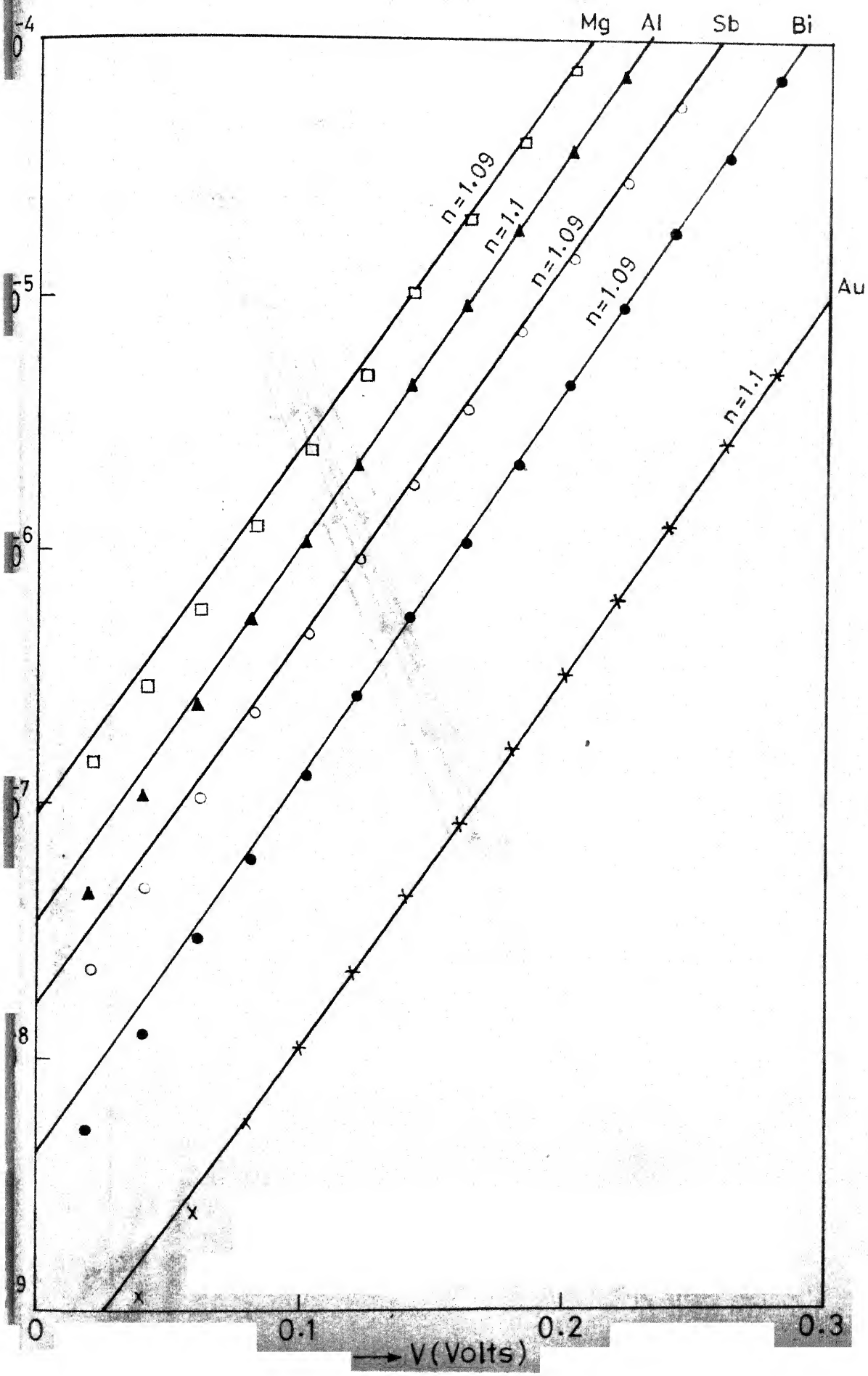
The measurements that were performed on these Schottky barriers included:

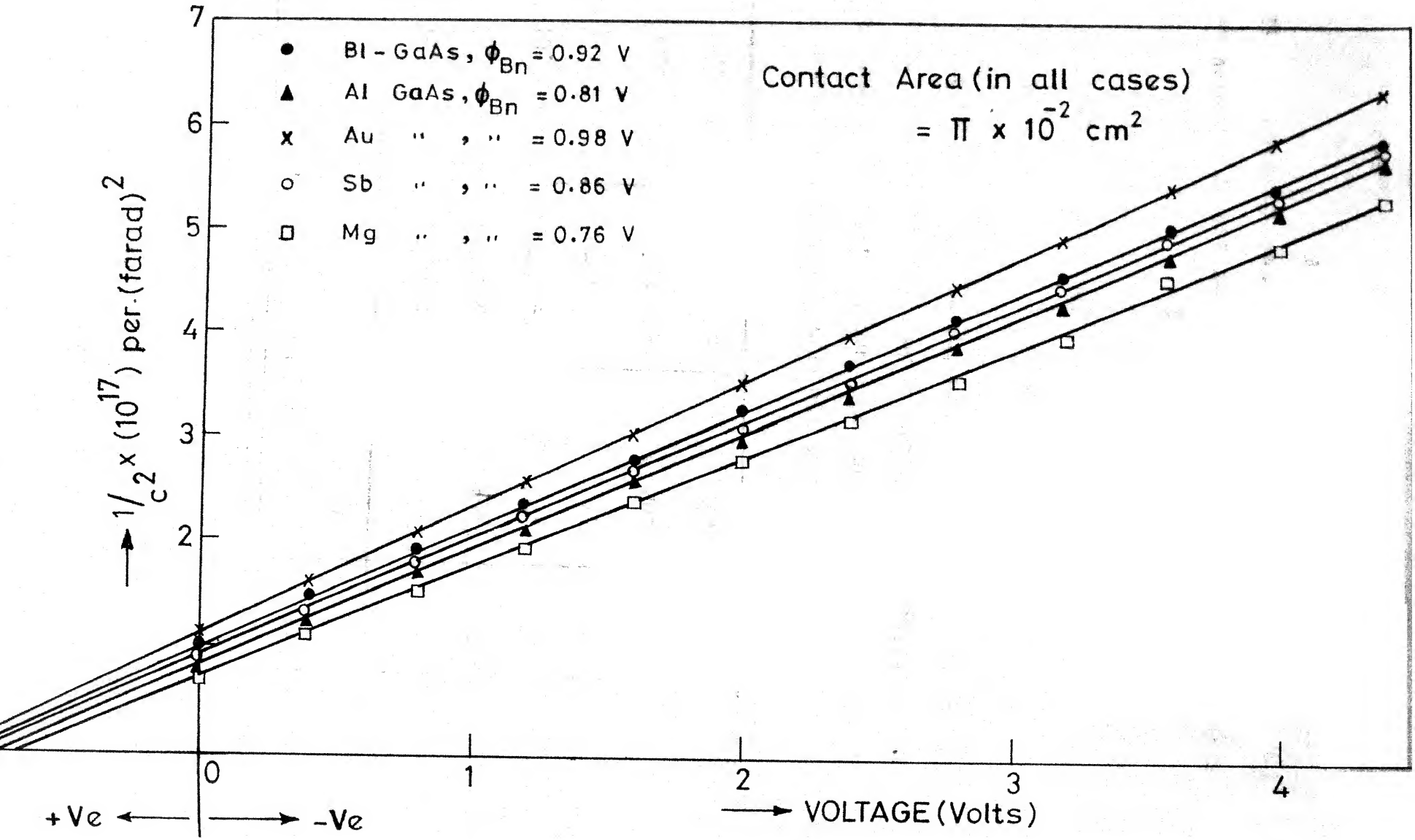
(i) Forward I-V characteristics, and

(ii) C-V measurement.

The details of these measurements have already been described in Section 5.2. Figure 5.9 shows the I-V characteristics and Figure 5.10 shows the C-V characteristics of these fabricated Schottky barriers.

The value of n has been estimated for all these Schottky barriers using the I-V characteristics whereas the barrier height has been calculated using the C-V


Mg
Al
Sb
Bi
Au
n=1.09
n=1.1
n=1.09
n=1.09
n=1.1
-4
-5
-6
-7
-8
-9
0
0.1
0.2
0.3
V (Volts)


Bl - GaAs, ϕ_{Bn} = 0.92 V
Al GaAs, ϕ_{Bn} = 0.81 V
Au " , " = 0.98 V
Sb " , " = 0.86 V
Mg " , " = 0.76 V
Contact Area (in all cases)
= π x 10⁻² cm²
$1/C^2$ x (10^{17}) per (farad)^2
VOLTAGE (Volts)
+Ve
-Ve
0
1
2
3
4
5
6
7

characteristics. These calculated values are tabulated along with the values of the work functions of various metals in Table 5.4.

TABLE 5.4: BARRIER HEIGHTS ON GALLIUM ARSENIDE

S.No.	Metal	Work function of the metal[5], ϕ_m	Contact area cm^2	ϕ_{Bn}(eV) from C-V measurement
1	In	3.8	$\pi \times 10^{-2}$	0.84
2	Bi	4.62	$\pi \times 10^{-2}$	0.92
3	Al	4.25	$\pi \times 10^{-2}$	0.81
4	Au	5.4	$\pi \times 10^{-2}$	0.98
5	Sb	4.02	$\pi \times 10^{-2}$	0.86
6	Mg	3.65	$\pi \times 10^{-2}$	0.76

Figure 5.11 shows the curve between the barrier height and their corresponding work functions. In this figure the data obtained from fabricated Schottky barriers has been fitted to a straight line and the result obtained is:

$$\phi_{Bn} = 0.079\ \phi_m + 0.52 \qquad (5.1)$$

When equation (5.1) is compared with equation (3.14), we get

$$C_2 = 0.079 \; ; \; C_3 = 0.52$$

Taking electron affinity to be 4.07 eV and $\delta\phi = 0.035$V at zero bias and using equations (3.14) and (3.12), we obtain

$$D_s = 1.29 \times 10^{14} \text{ states/cm}^2\text{/eV}$$

and $$q\phi_o = 0.48 \text{ eV}.$$

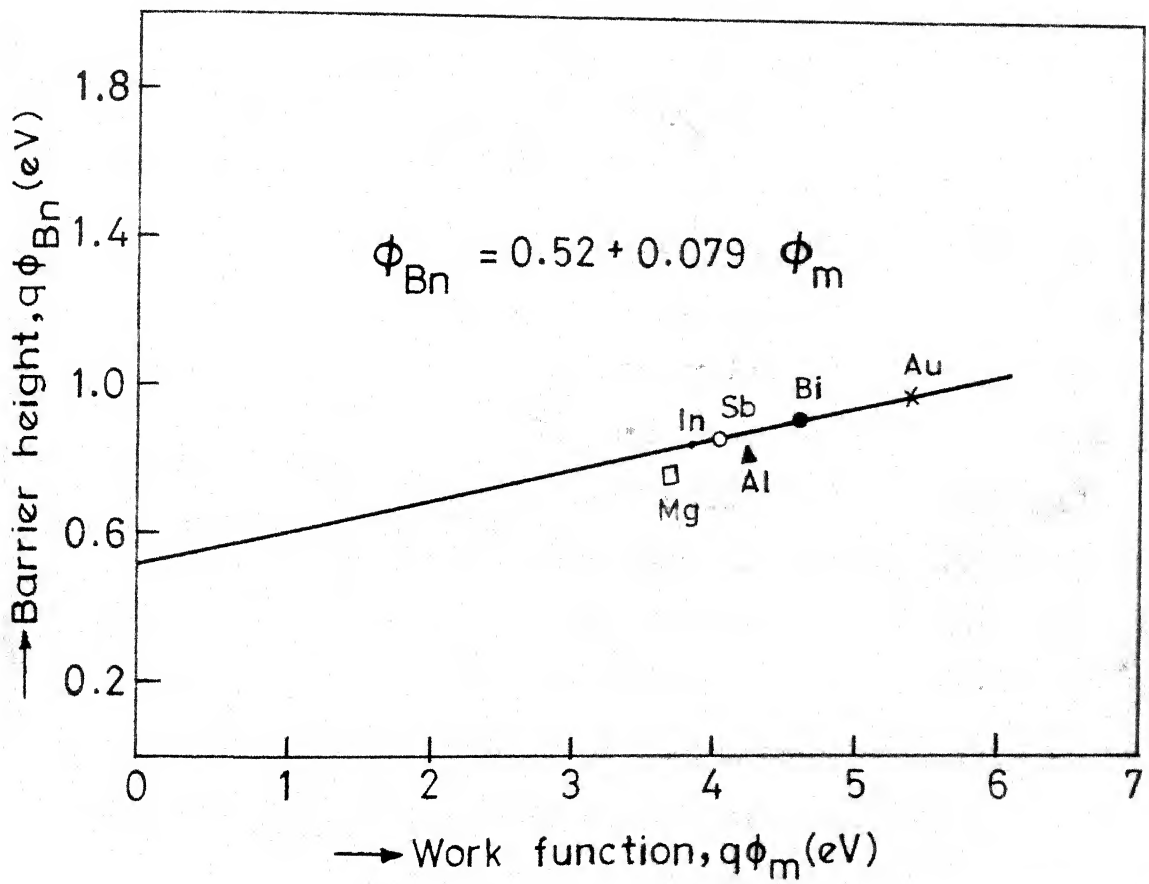


Fig. 5.11 Work function, ϕ_m, Vs Barrier height, ϕ_{Bn}, plot

5.5 DISCUSSION

The I-V characteristics of In-GaAs Schottky barriers exhibit values of n slightly more than unity as can be seen from Figure 5.1 and Table 5.1. This eliminates the possibility of the presence of any thick insulating layer between the metal and semiconductor, and confirms that the observed characteristics are that of a true Schottky barrier. The results in Table 5.1 are deduced assuming no space charge recombination current, no tunning current[6] and also the absence of minority carrier injection. In determining the value of barrier height, theoretical value[7] of A^* has been used in equation(3.24). This theoretical value of A^* may be slightly different from the value obtained by experimental measurements. (The use of the theoretical value of A^* rather than an experimental one has one advantage[7], that is : If one measures A^* and ϕ_{Bn} by plotting $\ln(J_s/T^2)$ vs. q/kT, when ϕ_{Bn} is temperature dependent, the apparent value of A^* that emerges is really $A^* \exp(-\frac{q}{k}\frac{d\phi_{Bn}}{dT})$ and the apparent barrier is that extrapolated to 0^oK. One is then forced back to the position of assuming a value of A^* to deduce ϕ_{Bn} at a given temperature unless a direct measurement of $d\phi_{Bn}/dT$ is available). Since the prediction of A^* is probably accurate within a factor[8] of e, however, this represents a possible error of the order of kT/q in ϕ_{Bn} measured by I-V characteristics.

The linearity of C-V curve indicates the existence of abrupt function in the In-GaAs diodes. The agreement in the values of barrier height obtained by I-V and C-V data is only qualitative whereas the agreement between the donor concentrations determined by capacitance measurement and that determined by Vander Pauw technique, however, is satisfactory.

Several factors that may effect the accuracy of barrier height obtained by C-V method have been discussed by Goodman[9]. Some of these factors that might have influenced the barrier height in our work are :

(i) a fixed resistance representing the semiconductor bulk resistance placed in series with the parallel combination of voltage dependent capacitance and voltage dependence conductance at the interface. This series resistance may effect the barrier height,

(ii) the existence of traps in the depletion layer. Since C-V measurements have been made while some light was incident on the metal surface, this incident light can cause either the optical excitation of trapped electrons to the conduction band or recombination with the optically generated holes. If the measurements are made in dark, the value of capacitance at zero bias may change because these traps will start getting refilled by the electrons, and

(iii) the correction factor employed in equation (3.28) may not be exactly kT/q.

The value of ϕ_{Bn} obtained by photoresponse is considerably larger than that calculated from the I-V plot but differs only slightly from the value deduced by C-V measurement. As has been mentioned above the interpretation of I-V data involves uncertainty in A^* and also in the observed value of n. These may very well be responsible for the consistently lower values obtained by I-V data. A careful examination of the reported data on GaAs Schottky barrier diodes shows[10] that for all the metals excepting tungesten the barrier heights as determined by the photoelectric method are smaller than that obtained by C-V method. In case of In-GaAs barrier, however, the opposite is true. As there are no other published data on In-GaAs contacts, no comparison can be made.

Figure 5.5 shows the experimental and theoretical values of barrier lowering as a function of applied reverse bias. The theoretical curve, which has been drawn considering only the image force lowering of the barrier and using equation (3.30) to calculate the barrier lowering when the image force dielectric constant equals the static value of dielectric constant, shows much smaller barrier lowering compared to the experimental values. Though the theoretical values of the barrier lowering could be higher, if surface states were also taken into account[11], the experimental values still seem to be higher than expected. From the slope of the experimentally determined curve in Figure 5.5, the image force dielectric constant, ϵ_d, was calculated and was found to be much smaller than the static value of GaAs.

The difference in the slopes of the theoretical and experimental curves in Figure 5.5 may perhaps be due to leakage current. In our experiment enough care was taken to eliminate the effect of leakage current on the photoresponse, but as measurements were made without any guard ring structure, it is possible that the value of proportionality constant K in equation (3.30) might have changed with voltage. An additional effect which might cause the barrier lowering to be much more than the value predicted by theory, is the existence of the traps[12]. Trap density of a good quality GaAs runs in the neighbourhood of 10^{16} traps/cm^3. Thus the effect of these trapping centers should certainly be considered. However, the exact role of these traps is not yet clear.

Forward characteristics, which have been studied at temperatures ranging from 243°K to 353°K show that the value of parameter n is temperature dependent. From Figure 5.8 one can see that value of n gets closer and closer to unity as the temperature is increased above the room temperature, and goes on increasing appreciably above unity as the temperature is decreased below room temperature. According to the basic theory n is given by[13]

$$n = \left[1 + \frac{\partial(\partial\phi)}{\partial V} + \frac{kT}{q} \frac{\partial(\ln A^*)}{\partial V} \right]^{-1} \qquad (3.23)$$

Thus when the temperature is varied in equation (3.23); (i) the value of A^* may change because the effective value of Richardson's constant is dependent on the effective mass

which itself may change because of the change in temperature, and (ii) the barrier lowering may change due to change in image force dielectric constant. In addition to these effects the depletion layer recombination current may also change with temperature.

In Figure 5.11, the work function ϕ_m vs. the barrier height for various metal-GaAs Schottky barriers is plotted. Referring to this figure, we notice that the experimentally determined points are scattered around the most probable straight line. A possible explanation for this deviation from a straight line is that the various Schottky barriers have been fabricated under different surrounding atmospheric conditions though same cleaning procedure was adopted in all the cases. Its effect could give rise to different thicknesses of interfacial layer δ in different Schottky barriers with the result that these Schottky barriers are near ideal in varying degrees. Another reason which can be thought of is that the barrier heights have been determined from the C-V measurement only which itself is not a very accurate method of measurement for the reasons explained earlier. Finally, published values of the work function, ϕ_m, for different metals have been used in Figure 5.11. These values themselves may not be very accurate because the metal work function varies with surface contamination.

The Fermi level ϕ_o at the surface has been calculated to be roughly one third of the band gap of GaAs. This value seems to be agreeing with the findings of Mead and Spitzer[14]. According to Mead and Spitzer when the density of surface states is substantially high as is the case with GaAs, the Fermi level tends to become pinned at the surface $q\phi_o$ eV above the valence band edge and produces a barrier height of $(E_g - q\phi_o)$ or $\frac{2}{3}E_g$. Our results seem to be agreeing fairly satisfactorily with this theoretical interpretation.

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Chapter 6

CONCLUSIONS

Schottky barriers on gallium arsenide have been prepared by the vacuum evaporation of Indium onto chemically prepared n-GaAs. Ohmic contacts to the samples of GaAs fabricated by the evaporation of In-Au composition (90:10 percent by weight) and subsequent alloying at 550°C for 30 seconds, are uniform, stable and having low contact resistance. This has been verified by the voltage-profile measurement performed on these ohmic contacts. Through these ohmic contacts are reproducible if alloying is done properly, there is one disadvantage with them. That disadvantage is the formation of an intermetallic compound In_2Au after the alloying which makes the contacts quite brittle.

The current in the fabricated In-GaAs Schottky barriers can be described by

$$I = I_s(e^{qV/nkT} - 1)$$

where the parameter n is found to vary from 1.06 to 1.1. Values of n have been seen to be temperature dependent. The qualitative reasoning for the temperature dependence of n is clear but quantitative formulation is warranted. However, no efforts have been made to compare the experimental results with theory.

Barrier heights of the fabricated In-GaAs Schottky barriers have been determined by I-V characteristics, C-V method and photoelectric method. The values of ϕ_{Bn} obtained by these methods are in fairly good agreement and confirm that the barriers are true Schottky barriers. Photoelectric measurements on these Schottky barriers have also been used to calculate the image force dielectric constant of GaAs. Considerable deviation between the experimentally determined values of barrier lowering and those determined by theoretical calculations has been observed. This deviation may partly be attributed to the leakage current and partly to the interfacial traps. It appears that interfacial traps play a dominant role though their exact nature is not yet clear.

The density of surface states and their position in the forbidden gap has been evaluated by fabricating Schottky barriers using five more metals, namely, Au, Al, Bi, Mg and Sb, and determining the barrier heights for all these Schottky barriers. When barrier heights were plotted against the work function of metals a straight line $\phi_{Bn} = 0.079\phi_m + 0.52$ was obtained. The value of the density of surface states, calculated from the slope and intercept of this straight line, is of the order of 10^{14} states/cm^2/eV and the position of the Fermi level at the surface is found to be at about one third the band gap above the valence band.

Indium is an inexpensive metal. With the relatively simple method of fabrication, In-GaAs Schottky barriers may have good prospects for commercial applications, though a more detailed set of measurements is desired before any more comments can be made. The only disadvantage with these Schottky barriers is that they cannot be used at higher temperatures because of the low melting point of Indium.

APPENDIX A

DETERMINATION OF IMAGE FORCE BARRIER LOWERING

For a metal the minimum energy required to take an electron from the Fermi level into vacuum is called the the work function ϕ_m. If we consider an electron at a distance x from the metal, the electron is attracted by the image charge and the potential energy at a distance x is given by

$$\mathcal{E}(x) = -q^2/16\pi\epsilon_0 x)$$

In an applied electric field E the potential energy of an electron at a distance x is -qEx. Thus in the absence of an applied electric field the total potential energy of an electron will be

$$P_E(x) = -(qEx + q^2/16\pi\epsilon_0 x)$$

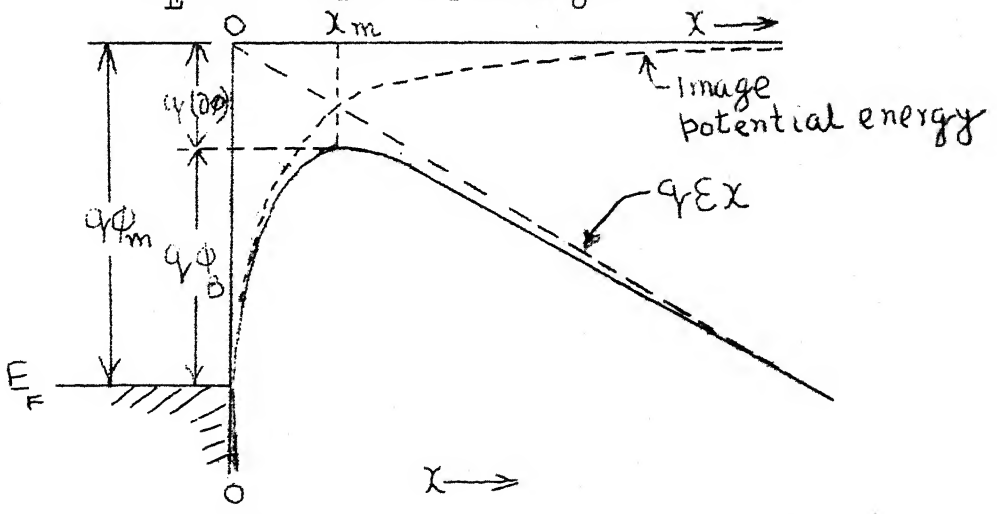


Figure A.1 Energy diagram between a metal surface and vacuum.

These energies are plotted as a function of x in Figure A.1. The energy $P_E(x)$ will be maximum when

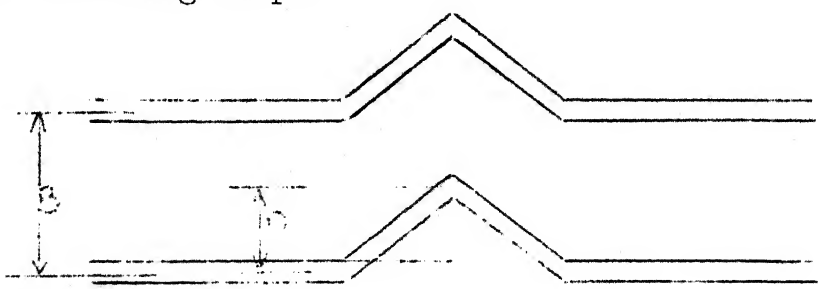
$$dP_E(x)/dE = 0$$

APPENDIX B

DETERMINATION OF THE FILM THICKNESS

The thickness of the evaporated layers is found out by the unitron microscope. The procedure of the measuring the thickness using the interference frings is as follows:

Interference frings exist at the portion of the shinning specimen where the evaporated layer edge exists. These are observed under the unitron microscope and are of the following shape:



B = Distance between interference bands or frings.

D = Deflection of the band.

Measure the distance B between the centers of adjacent bands using the linear eyepiece micrometer. Next measure the amount of deflection D. The depth of the disturbance is equal to D/3B microns.

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